POWER ELECTRONICS WORLD

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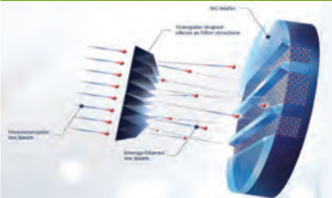
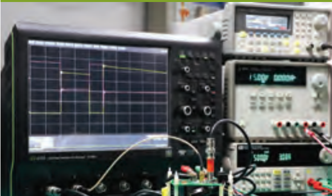
The rise of GaN-based power systems

Addressing SiC super-junction MOSFETs



Rohm braves high voltage SiC markets

Obliterating dynamic on-resistance degradation



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Viewpoint

By Mark Andrews, Technical Editor

Power electronics growth may outpace other semiconductors in 2019

AS THIS EDITION of Power Electronics World finalizes, semiconductor makers serving broad markets are recording mixed results after 2018's record-setting pace. Meanwhile, researchers studying power electronics device manufacturing see positive signs driving 2019 revenue prospects.

According to the SEMI trade group, 2018 was a great year for broad markets—chip revenue topped (USD) $469 billion compared to 2017's $412 billion, up about 12 percent. Yet 2019 shipments of silicon wafers are down compared to 2018 and 2017 records. The cyclic nature of memory sales is continuing, with Micron Technologies and Samsung Electronics both indicating they expect lower results for the current quarter than initially forecast. For 2018, SEMI reported that manufacturing equipment and materials suppliers celebrated as sales hit record levels of $65 billion and $52 billion respectively, calling 2018 'a remarkable industry trifecta' since chip, equipment and materials sales all logged a third consecutive year of growth. That hasn't happened since the mid-1990s, but early indicators say 2019 will be hard pressed to extend that run.

Prospects for power electronics manufacturers look much better. Due to the push to convert petrol and diesel-fueled automobiles and trucks to hybrid or full electric vehicle (EV) designs, researchers find more optimism amongst power device manufacturers. Allied Market Research predicts growth of 8.9 percent through 2022, pushing the market to (USD) $25 billion, while Market Watch researchers say the power electronics market will grow to $45 billion by 2024.
In this edition of Power Electronics World, GaN Systems brings us Part II of its three-part series on GaN design tips. Gallium nitride devices are playing an increasingly significant role in automotive applications including EVs and hybrids thanks to

their greater ability to handle higher breakdown voltages at greater efficiencies.

Capacitors are also found throughout automotive systems, making our article from EEStor about its new glass-composition modified barium titanate (glass-CMBT) devices all the more timely. EEStor devices substantially reduce size, weight and cost while also dramatically extending the lifetime of capacitors in LEDs, automotive powertrains and renewable energy inverters. And imec provides an interesting look into its new approach for super-thin semiconductors needed in high voltage applications such as automotive powertrains and electric vehicle charging systems.

While SEMI reports mixed growth in broad 2019 semiconductor markets, remember that manufacturing is a 'long-game,' especially for automotive and general transport. The Robert Bosch Corporation broke ground in January for its new billion euro chip plant in Dresden set to double its in-house chip and sensor making capability by 2021. That's a vote of market confidence we all need to hear.

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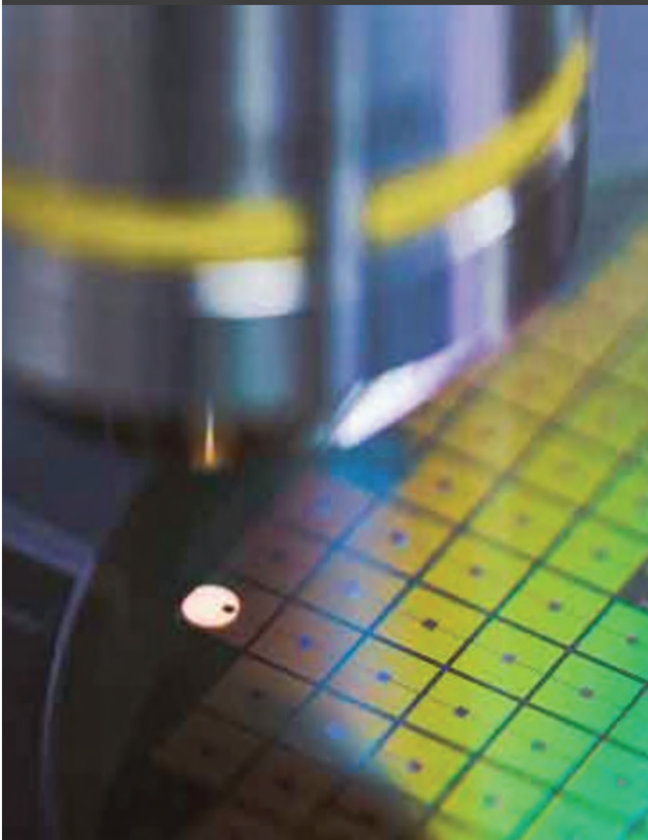

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Panasonic Technology portfolio: Solutions for automotive and industrial at PCIM, Germany

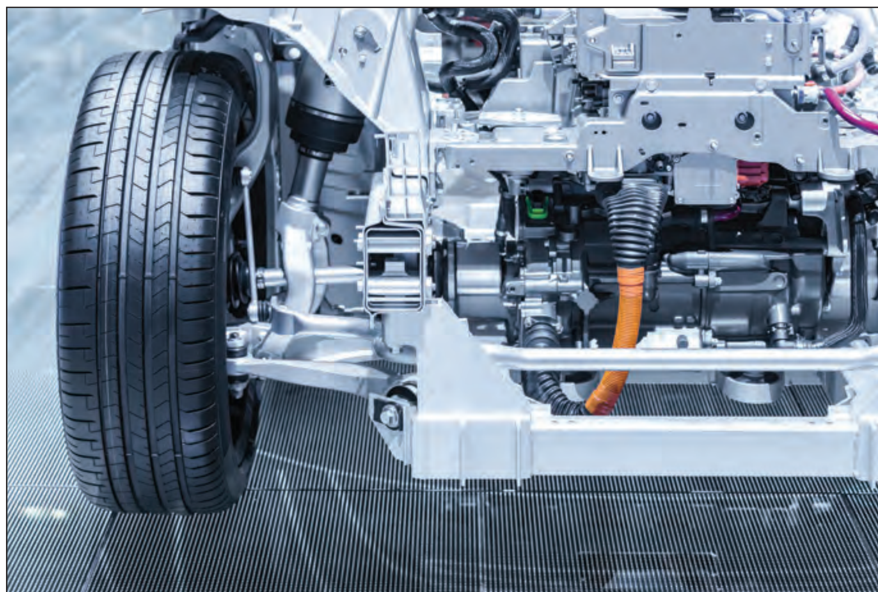
PANASONIC will present its latest technology portfolio at PCIM, Nuremberg. Strong innovations in the fields of wide bandgap semiconductors, assembly technology and passive components technology form the basis of Panasonic unique position as the solution partner addressing the broadest range of challenges of the modern power electronic design.

Panasonic X-GaN transistors provide superior switching performance and high reliability and robustness, thanks to their fast switching, highly conductive structure that suppresses current collapse.

hese benefits are demonstrated in new reference designs of a 3kW totem pole PFC and of a 65W active clamped flyback AC adapter.

Panasonic has developed a single chip GaN bi-directional switch capable of operating in 4 quadrants, by adopting an innovative dual gate device structure.

This device enables a significant reduction of conduction losses and of the number of components needed in topologies such as multilevel inverters, matrix converters and Vienna rectifiers.



Panasonic range of low inductive power modules for xEV drivetrain embed Panasonic's DioMOS (Diode-integrated) MOSFETs. The DioMOS structure enables a size reduction of SiC modules by integrated free-wheeling diode functionality inside the MOSFET.

GraphiteTIM is the next development step of the Pyrolytic Highly Oriented Graphite Sheet (PGS) portfolio. This PGS 100μm thin sheet acts as lightweight and easy to handle film with a thermal conductivity 700W/mK in plane and 26 W/mK out of plane.

GraphiteTIM has been developed as a thermal interface material and boasts a high thermal conductivity of 28 W/mK which effectively disperses and transfers heat along X, Y and Z axis, provides better compressibility of 40% €600kPa pressure, easy handling and high reliability over the whole product life. Passive components on display feature Conductive Polymer Hybrid Aluminum Electrolytic Capacitors, which enable high power applications to achieve optimum performance through their low ESR, high ripple long life characteristics.

Automotive film capacitors (AEC-Q200 compliant)- contribute to high safety & high reliability solution for a broad spectrum of application including automotive, industrial and renewable energy.

Metal Composite Power Choke Coils offer a unique combination of features – high current capability, high reliability and good anti-vibration characteristics – which enable application design flexibility.

Flex Power ultra-wide-input DC-DC converters

FLEX POWER MODULES introduces the PKE-A series of DC-DC power modules for the Industrial and Railways sectors, broadening its product range to meet increasing demand in these sectors. The modules are provided in sealed and encapsulated packaging, to ensure they will work reliably when subjected to dust, moisture, severe vibration and other harsh conditions.

For Industrial applications, the PKE8000A series provides highly reliable, high-performance and rugged DC-DC solutions in the industry-standard 2 x 1in form factor, running from 12V, 24V or 48V supply voltages thanks to its ultra-wide-input range of 9 to 75V.

Delivering up to 40W of output power at up to 91% efficiency, the series also offers mean time between failures (MTBF) of up to 4 million hours, and input-to-output isolation of 2250VDC. The devices meet the latest IEC/EN/UL62368-1 safety standards.

For Railways applications, the PKE7000A series is packaged in the same 2 x 1in industry-standard form factor, but this time operates from a 43 to 160V input, delivering up to 30W. This makes it suitable for the majority of onboard requirements running from 72V and/or 110V nominal supplies, most commonly found in the Railways sector. The devices comply with the EN50155 railway standard and offer MTBF figures of up to 5 million hours to satisfy the most demanding applications.

Both the PKE8000A and PKE7000A families are available now for sampling and volume production requirements.

Medical, 2 x MOPP, DC-DC converters simplify development of safety-critical medical devices

XP POWER has launched a new range of 20 Watt DC-DC power modules with international agency approvals for medical/healthcare applications. The series is suitable for all medical applications and particularly intended for use where the DC-DC converter provides a reinforced (2 x MOPP) safety isolation barrier, including patient contact and patient vicinity applications.

Modules in the JHM20 series are certified by both UL & TUV and carry all international approvals including IEC60601-1, EN60601-1 and ANSI/AMMI ES60601-1 for medical safety. This certification, and with the CB report including risk management, allow designers to use them for critical safety barriers with confidence, while reducing the time and cost associated with the end equipment approval. Suitable for direct patient contact, the modules have a maximum of just 2.5μA of patient leakage current and offer 2 x Measures of Patient Protection (MOPP) at a 250VAC working voltage, ensuring patient and operator safety.

The JHM20 series comprises a total of 18 modules, offering 20 Watts of power in a compact 50.8mm x 25.4mm PCB-mount footprint. The 2:1 input range offers flexibility with nominal input voltages of 12, 24 and 48VDC. Isolated, fully-floating, single and dual output versions are available at 5, 12 and 15VDC, allowing the provision of single rails of 24 and 30VDC. All single outputs are simple to trim by ±10% via a single external resistor.

The modules offer excellent levels of efficiency and operate from -40°C to +80°C, delivering full power at temperatures up to +60°C allowing use in challenging applications. A wide range of protection mechanisms such as short circuit and overload are included to protect both the power module and the system load. The case is made from a self-extinguishing UL94V-0 material. JHM20 modules are certified to meet the EN55011 Level A standard for EMC emissions without the need for any external components. It is also certified to IEC60601-1-2 Ed. 4 for EMC immunity. These pre-certifications ease the task of the designer when submitting for system-level approvals.

The JHM20 series is available from Allied Electronics, Digi-Key, element14, Farnell, Newark, RS Components, approved regional distributors, or direct from XP Power and come with a 3-year warranty

STMicroelectronics' 650V IGBTs boost performance

THE STMICROELECTRONICS HB2 650V IGBT series delivers efficiency and performance gains for medium- and high-speed applications such as PFC converters, welders, uninterruptible power supplies (UPS), and solar inverters, leveraging ST's latest Trench Field Stop (TFS) technology. The series also includes automotive-eligible devices meeting AEC-Q101 Rev. D.

Joining the STPOWER portfolio, the new HB2 series has outstanding conduction performance thanks to low VCEsat of 1.55V. At the same time, dynamic behaviour is enhanced due to reduced gate charge that enables fast switching at low gate current. Outstanding thermal performance helps maximize reliability and power density, while the new products are also positioned as a very competitive choice in the market.

The HB2 series IGBTs can be specified with either a full-rated or half-rated diode, or a protection diode to prevent accidental reverse bias, giving extra freedom to optimize the behavior for specific application needs.

This package is designed for use in space-constrained applications power conservation is critical. The LIS2D2DTW12 has four user-selectable full acceleration measuring scales: ±2g/±4g/±8g/±16g. 16-bit output rates can range from 1.6 Hz to 1600 Hz. There are a total of 65 user modes that enable designers to control the unit's power consumption.
It is configured to detect if the device it's built into is in portrait or landscape orientation (4D orientation). It also has 6D orientation capability, which provides more detailed information about the device's spatial position.

The unit offers configurable recognition between single-taps and double-taps. It can also detect freefall and motion used to tell the device when to "wakeup" from a sleeping/low power mode. Temperature sensing is accomplished with output data rates (ODRs) ranging from 50 to 1.6 Hz and resolution from 8 to 12 bits.

To enhance the overall speed of system operation, the unit has an integrated 32-level first-in, first-out (FIFO) buffer. This allows the LIS2D2DTW12 to store data internally in order to limit intervention by the host processor.

Communication is accomplished through an SPI (Serial Peripheral Interface) or an I2C (inter-integrated circuit) interface.
The first of the new 650V devices, the 40A STGWA40HP65FB2, is available now in the TO-247 long-lead package, priced from $2.95 for orders of 1000 pieces.

Vishay Siliconix and TowerJazz expand manufacturing collaboration

TOWERJAZZ and Vishay Siliconix has announced manufacturing portfolio expansion of existing and next-generation power semiconductor products for the automotive markets, to be produced in two of TowerJazz's worldwide IATF16949 qualified manufacturing facilities. The newly developed automotive dedicated platforms will enable improved efficiency of power management circuitry in end products while reducing space requirements.

"With the ongoing increase of electronic content, automotive has been the main driver of growth in our industry. Ranking as Vishay Siliconix's number one foundry while continuously supporting growing market activities, this expansion recognizes TowerJazz's valuable continued commitment, exceptional technical and customer support, strong collaboration, and delivery performance," said Serge Jaunay, Vishay MOSFET Division Head.

According to IC Insights, the automotive IC market reached record revenue of $32.3 billion in 2018 and is expected to remain the fastest growing IC market with a CAGR of 12.5%, exceeding $43 billion in 2021. This market is expected to be dominated by analog ICs, power management including power MOSFETs, visual and non-visual sensors, RF, and lighting.

Vishay Siliconix utilizes TowerJazz's Transfer Optimization and development Process Services (TOPS) business unit for its world-leading low-and high-voltage power MOSFET products. These services provide best-in-class transfer methodologies, including the development of next-generation custom processes, technological capabilities with manufacturing capacity assurance and flexibility.

"We are excited to expand our long-term collaboration and business relationship with Vishay Siliconix, our highly valued customer and partner. The combination of both companies' extensive technology expertise and market leadership, fosters an environment allowing mutual growth and success, enabling us to best serve Vishay Siliconix's technological and operational needs", said Zmira Shternfeld-Lavie, Senior Vice President and General Manager of Transfer, Optimization and development Process Services (TOPS) Business Unit.

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EEStor capacitors

offer cost, space advantages

The world is generating and using more renewable electricity than ever before, but in many cases, that electricity is still being generated by intermittent sources including solar and wind. While these renewable technologies are undoubtedly central to a decarbonized future, they can't generate power all the time (yet), causing gaps in supply.

By Ian Clifford, founder and CEO of EEStor Corporation

WITHOUT A DOUBT, the biggest issue in renewables is how to create 'fit for purpose' energy storage solutions. If we have no cost effective or scalable way of storing the energy we are generating, then we have no way of controlling time of use or distribution through the grid. What if we could store renewable electricity from intermittent sources, even when they aren't able to generate, enabling us to use their output on demand and at electronic speeds?

Enter EEStor Corporation. We provide leading edge, solid state electrical energy storage solutions and related technologies. Our primary technology is an innovative solid-state electrical storage technology that is set to disrupt the current US $4.6bn (~€3.93bn) aluminum electrolytic capacitor (AEC) global market.

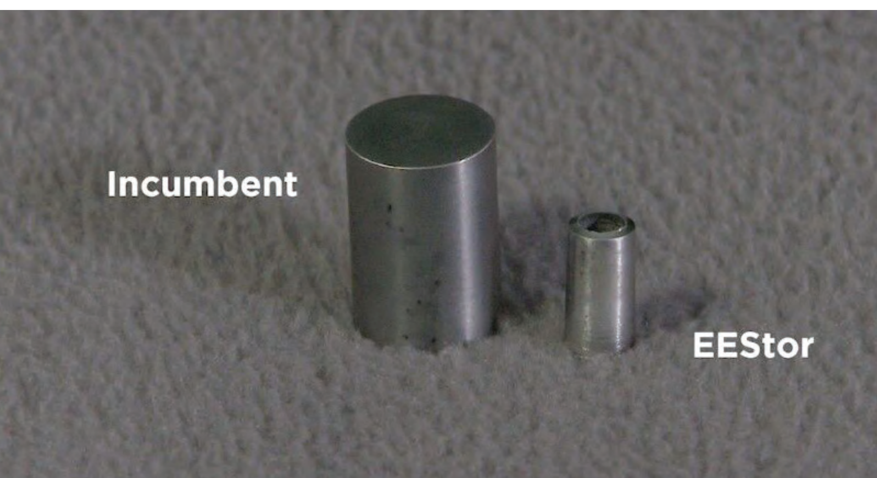

Figure 1: Incumbent capacitor size (left) compared to the EEStor version for the same-size application (right). Photo by EEStor.

Our unique hybrid capacitor dielectric material – glass-composition modified barium titanate (glass-CMBT) – has been shown in independent third-party testing to provide higher permittivity at a significantly reduced cost to existing capacitor technologies. As a result, our replacement capacitors use up to 86 percent less material than incumbent aluminum electrolytic capacitors (AEC).

Capacitors based on EEStor technology could be used in many renewable energy applications to extend the life and lower the cost of ownership. Some applications that would benefit from EEStor's longer life / lower cost of ownership technology are LED lighting applications, DC-link and snubber capacitors for inverters in wind and solar as well as transportation sectors and in smart grid applications. Details of the benefits of EEStor technology for these applications can be found in the following case studies: LED Case

Capacitor - voltage, size	40V, 33 µF	450V, 10 µF	450V, 470 µF	500V, 2.9 µF
Type	AEC	AEC	AEC	MLCC
Kemet Volume	1.57 cm^3	5.83 cm^3	-	2.46 cm^3
United Chemi-Con Volume	-	-	43.3 cm^3	-
EEStor Volume	0.874 cm^3	0.811cm^3	38 cm^3	0.33 cm^3
% larger than EEStor	80%	618%	14%	645%

Table 1: Size comparison of various capacitors*

Study, DC-Link Case Study and Electromagnetic Compatibility Systems Case Study

Incumbent AEC's also have comparatively short expected lifetimes, but with our new dielectric material, our licensees and partners can build capacitors that dramatically extend current AEC lifetimes from thousands and tens of thousands of hours, to decades.

An alternative to aluminum tantalum and plastic film-based capacitors

EEStor's unique capacitors are cheaper per farad to manufacture due to our use of less expensive materials, resulting in less material cost for each farad. Our ceramic based capacitors also have lower cost feedstocks in barium carbonate and titanium dioxide, and since our capacitors contain little to no empty space, the volume of the final part is directly related to the volume of the material needed to construct them. To help illustrate this point take a look at the following image.

The above images show two cylinders. The larger cylinder is 5.8 cubic centimeters and is the exact same size as an incumbent 450-volt 10 micro farad capacitor. The smaller cylinder is 0.8 cubic centimeters, which is the same size as the EEStor 450-volt 10 micro farad capacitor. As you can see, the larger cylinder representing an incumbent capacitor is significantly larger; in fact it is 618 percent bigger than EEStor's version. However, our capacitor offers the same capacitance in this small volume as an aluminum electrolytic capacitors does in a much larger volume.

EEStor's composition modified barium titanite (CMBT) is blended with glass, forming a hybrid dielectric, as hybrid dielectrics have significantly higher permittivity than commercial dielectrics. This blend of EEStor designated Phase 7 & 8 materials has been tested extensively by three independent testing certification organizations - Intertek, Radiant Technologies and MRA. Information about testing laboratories and the performance details are contained in the following reports – Intertek phase 7, Radiant phase 7, MRA Phase 7.

Lighting utilizing light-emitting diode (LED) technology provides a great example of the lifetime issues associated with aluminum electrolytic capacitors. As Power Electronics World's readers will know, to be energy star rated LED lights must meet lifetime requirements. Current standards state that the emitted light intensity of the LED lights must not drop more than 30% in 25,000 hours of operation for residential applications, or thirty-five thousand hours of operations for commercial application.

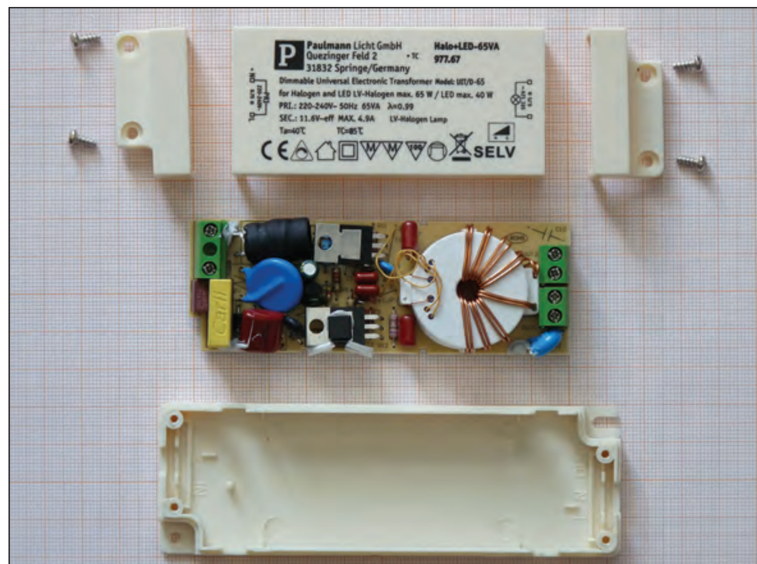

Figure 2: The above power supply could be utilized for any 56-watt LED load such as a LED street light, or other commercial high intensity LED lighting. Photo courtesy of Dimitry G / Paulmann Licht GmbH through CreativeCommons.org

displace incumbent markets for aluminum electrolytic capacitors in numerous markets including renewable energy applications for inverters in wind turbines, solar farms, ocean and wave generation, commercial aircraft, medical devices, oil and gas, electronics, communications infrastructure, electric rail and automotive electronics subassemblies.

Incumbent AECs and the EEStor alternative

Let's take a closer look at the current AEC market. In 2018 AEC's are expected to represent a (USD) $4.6 billion market globally. AEC's are utilized extensively in broad and diverse markets including alternative energy and LED lighting. In addition, AEC's are found throughout industrial telecommunications, automotive, military, medical and consumer electronics applications. In other words, AEC's are used throughout applications that touch almost every aspect of our daily lives. AEC's account for 6.5 percent of all capacitor shipments in terms of volume, but a full 22 percent of the global capacitor market in terms of US dollar value—a global market that is projected to reach 5.5 billion US dollars by 2022 by Global Industry Analyst.

This reduction by 30 percent is known as the L70 point. The typical high brightness LED circuit could last perhaps forty-five thousand hours before getting to the L70 point. The fundamental issue is that the lifetime of the typical LED power supply may only be twenty thousand hours, due to the failure of the aluminum electrolytic capacitor in the power supply. So, in the end, it doesn't really matter how long your LED light lasts if the power supply behind it can only last twenty thousand hours. EEStor technology could potentially enable a LED lamp to operate to its full rated life expectancy an increase of expected service lifetime of over 40%.

All aluminum electrolytic capacitors have lifetime issues, not just in LED lighting. EEStor's aluminum electrolytic replacements are significantly smaller, less expensive to produce and replace, and last longer. EEStor enables its licensees to manufacture capacitors that are substantially smaller, cheaper and that last significantly longer than aluminum electrolytic capacitors. Our savings on manufacturing cost and longer expected lifetimes combine to provide a significant advantage for this technology in the cost per farad per year. Replacing an aluminum electrolytic capacitor with an EEStor capacitor is also a straightforward process for an engineer.

As a result, when these products are on the market in the near future, we expect our licensees to

AEC's are known for high capacitance values, but unfortunately, as the LED example shows, they possess a limited operational lifetime, as the oxide layer degrades with time and temperature. By comparison, EEStor's capacitors are significantly smaller than aluminum electrolytic capacitors for the same capacitance and they have a much longer expected lifetimes.

EEStor's capacitors are much less expensive per farad, due to our lower cost of materials and higher volumetric efficiency and when costs are amortized over the lifetime of the devices the cost per farad per year is drastically improved over AEC's presently serving the market.

About EEStor
EEStor is a developer of high energy density solid-state capacitor technology utilizing the company's patented composition modified barium titanate (CMBT) material. The company is focused on licensing and joint venture opportunities for its technology across a broad spectrum of industries and applications.

*Capacitor comparisons are from EEStor Intertek Phase 8 and the following manufacturer specifications:
https://www.mouser.com/datasheet/2/212/KEM_A4011_PEG124-1104316.pdf,
https://www.digikey.com/product-detail/en/united-chemi-con/EKMQ451VSN471MA45S/565-3031-ND/758243, https://4donline.ihs.com/images/VipMasterIC/IC/KEME/KEME-S-A0002497309/KEME-S-A0002497309-1.pdf

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Balancing charges to boost performance

Incorporating a novel charge-balance drift region into a SiC Schottky barrier diode sets a benchmark for the key metric: on-resistance as a function of breakdown voltage

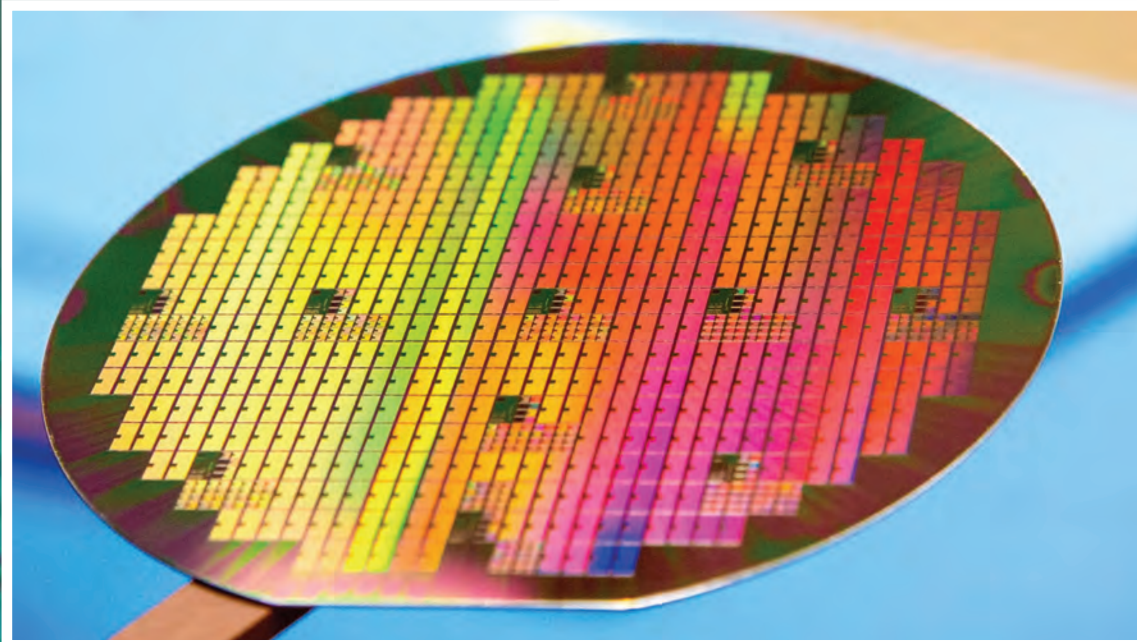
BY ALEXANDER BOLOTNIKOV, REZA GHANDI, PETER LOSEE, STACEY KENNERLY AND RAVISEKHAR RAJU FROM GENERAL ELECTRIC

THERE ARE SIGNIFICANT drawbacks associated with today's medium-voltage power conversion systems. These converters – installed on ships, used in wind turbines, fitted on solar farms and appearing in traction drives in transportation – are held back by a maximum switching frequency of no more than several hundred hertz. This limitation, stemming from solid-state switch and diode losses, dictates that the transformer, as well as the components for the converter filter, are very large and heavy. In turn, this leads to high costs for the system and its installation, and restrains design flexibility.

What's needed are highly efficient, lightweight power-conversion systems that can handle many megawatts while running at switching speeds of several kilohertz. Such converters are only a dream today, but they could become a reality if solid-state devices could switch at frequencies from one kilohertz to hundreds of kilohertz, while handling hundreds of amps.

Those that are developing these devices include our team at General Electric. Our successes to date include a SiC junction barrier diode with a novel, charge-balanced architecture that slashes conduction losses.

The benchmark for judging our devices is the incumbent technology in medium-voltage power conversion applications: silicon insulated-gate



GE is developing SiC Schottky barrier diodes with an impressive on-resistance for the given operating voltage

bipolar transistors (IGBTs) and diodes made by the likes of Infineon Technologies and ABB. In these bipolar devices, injected carriers are stored in the device's lightly doped blocking layers. In the on-state, these carriers increase the background carrier concentration, and enable a low forward-voltage drop (see Figure 1). And in the blocking-state, high voltages are possible, thanks to drift layers that are hundreds of microns thick and doped to levels of just 10^{13} cm^{-3}. For silicon IGBTs, these layers can lead to a blocking voltage as high as 6.5 kV.

The penalty to pay for these stored carriers in high-voltage silicon power devices is extreme losses, even at switching speeds of just 1 kHz. Consider, for example, a silicon IGBT module designed to handle up to 6.5 kV and 400 A. It has a turn-off loss of 2.1 J, equating to 1 kW of dissipation for switching at 500 Hz.

Note that designers of these modules are not just trying to minimise this switching loss. Their overriding goal is to find the sweet spot between realizing low switching losses and a low conduction loss. So, for example, in modules made by ABB the on-state voltage ranges from 2.7 V to 5.4 V, well beyond the entitlement for a silicon turn-on voltage of 0.7 V. This high on-state voltage is chosen to ensure switching loss reduction, but it constrains current density to typically between 30 A/cm² and 60 A/cm².

Yet another limitation stems from the high on-state voltage drop associated with the bipolar devices' *p-n* junction. This drags down converter efficiencies under partial load operation.

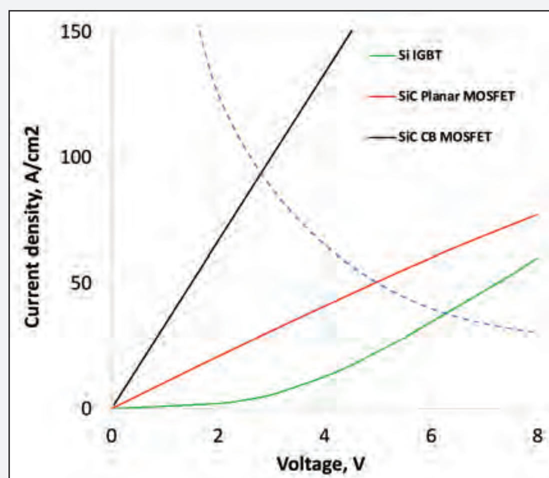
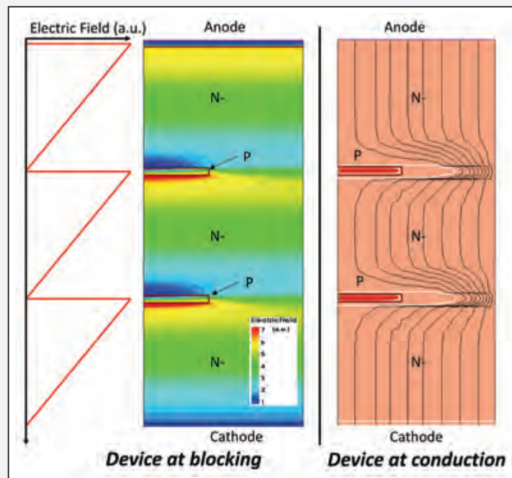


Figure 1. Comparison of typical forward characteristics of 6.5 kV devices at 125 °C. The SiC charge-balanced (CB) MOSFET offers a relatively high current density for a given forward voltage.



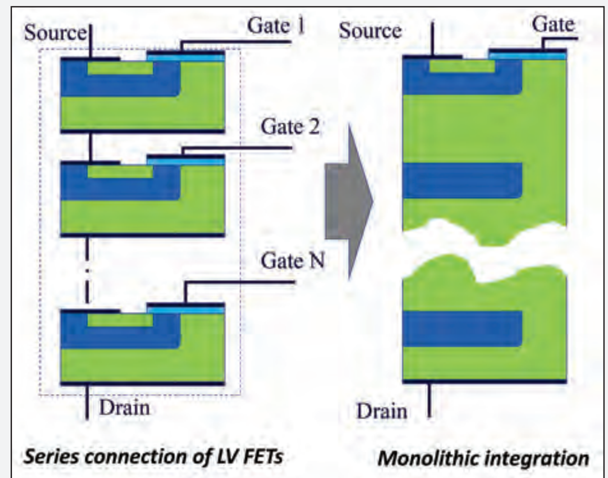


Figure 2. The operation (a) and design (b) of the charge-balance device.

The solution to all these problems is to turn to wide bandgap power switches and diodes. Devices made from GaN and SiC promise far lower switching losses and more efficient power conversion in a wide range of applications. What's more, for lower-voltage applications – that is those between 650 V and 2.5 kV – SiC devices also tend to operate with lower conduction losses.

However, when it comes to the devices typically deployed in medium-voltage converter applications, SiC is currently failing to fulfil its potential. One issue is that the conduction loss found in the drift layers of SiC unipolar devices is, at elevated temperature, often only marginally better than that of silicon IGBTs and diodes – and it can be even worse. Compounding matters, in SiC IGBTs, the large bandgap leads to an on-state voltage drop of more than 4 V at all operating current densities. And last but by no means least, the low current densities in SiC MOSFETs, IGBTs, and diodes results in the need for large die areas for handling the power levels required for megawatt applications. This is bad news, as it exacerbates chip costs.

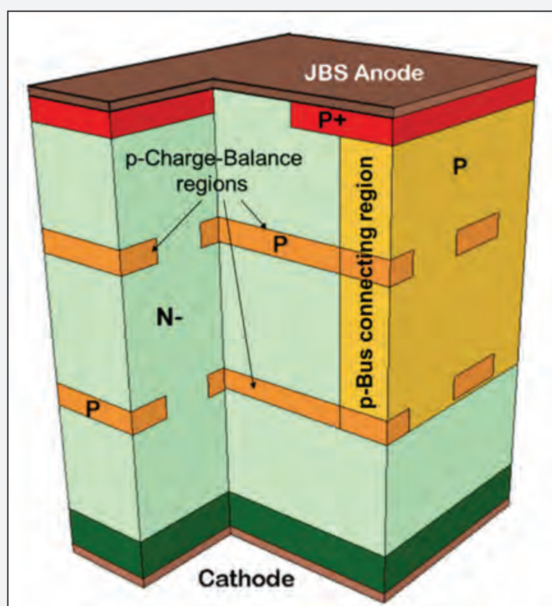


Figure 3. Engineers at General Electric are pioneering the SiC charge-balance junction-barrier Schottky diodes. They feature p-charge balance and p-connecting regions.

Two options for addressing the decline in the performance of SiC devices at increasing voltages are the series connection of lower-voltage devices, and drift layer engineering that utilizes 'superjunction' technologies. The latter is preferred, as it does not require multiple devices. Instead, it features a drift/blocking region that consists of multiple, alternating *n*- and *p*-type doped pillars with a relatively high doping that allow a high breakdown voltage. This is in stark contrast to the standard approach for realising a high blocking voltage: a single, lowly and uniformly doped blocking region that when depleted results in a nearly uniform electric field distribution in the drift region.

Several groups, including that headed by Paul Chow from Rensselaer Polytechnic Institute, have modelled the SiC superjunction vertical power device. But the realisation of these devices has remained elusive until now. While trench and refill approaches have garnered some interest, it is challenging to realise high aspect ratios, doping controllability, and scalability to higher voltages. These barriers have held back the experimental demonstration of a fully functional device.

We have broken through, by addressing the key challenge of achieving deep/high-aspect-ratio pillars of dopants in SiC superjunction devices with a novel, yet practical, SiC charge-balance drift region architecture. Armed with this technology, we have produced the first ever SiC junction-barrier Schottky diode.

How does charge-balancing work?

In our devices, the buried *p*-type charge-balance regions compensate for the higher *n*-drift doping concentration under reverse bias (see Figure 2). When the charge-balance regions are designed correctly, they act as electric field dividers, allowing an increase in doping in the drift region for a given breakdown voltage. The upshot is a reduction in conduction losses. Note that this concept is very similar to that of the serial connection of low-voltage devices that are monolithically integrated on the same chip.

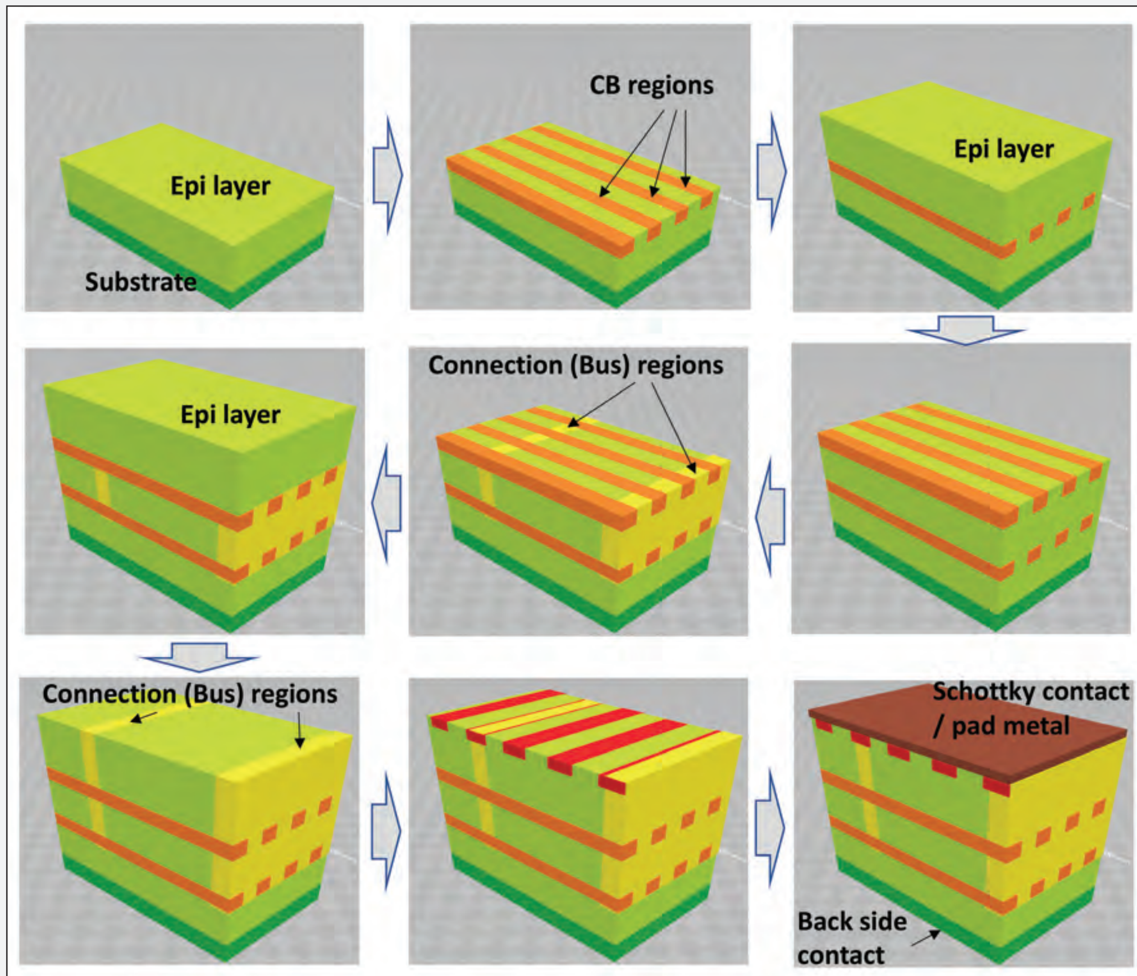


Figure 4. Several steps are required to fabricate SiC charge-balance junction-barrier Schottky diodes.

The drawback of such a structure is its poor dynamic response. The charge-balance regions require holes in the *n*-type drift layer to transition from blocking to conduction. Unfortunately, this cannot occur quickly enough when relying only on the recombination-generation rates of the carriers. To alleviate this bottleneck, our design also employs *p*-Bus connecting highly doped *p*-type regions (p^+) of the planar device to each of the charge-balance regions (see Figure 3). This refinement allows holes to flow into and out of the charge-balance regions during switching events.

The challenge with our architecture is to make the *p*-Bus connecting region sufficiently narrow, and with low enough doping, to minimize the alteration of the electric field distribution of the charge-balance drift region; but to make this region conductive enough to establish a good connection between the p^+ and charge-balance regions.

We have exceeded in this endeavour with our 2 kV and 3 kV SiC charge-balance, junction-barrier Schottky diodes, which were fabricated from 4H-SiC wafers with 10 μm-thick epitaxial layers doped at 1×10^{16} cm^{-3}. Our fabrication process began with the formation of *p*-type charge-balance regions fabricated by ion implantation of aluminium. After this, we undertook additional epigrowth, before adding *p*-connecting regions via high-energy implantation of aluminium using Tandem Van de Graaff facility at Brookhaven National Lab.

Our 2 kV diodes feature two 10 μm-thick epilayers and a single charge-balance region, while their 3 kV

Our results show that SiC Schottky barrier diodes with a novel architecture featuring a charge-balanced drift region can break the one-dimensional limit for on-resistance as a function of breakdown voltage. This success should pave the way to medium-voltage-class SiC unipolar switches with on-state and dynamic losses that are well below those of their silicon counterparts.

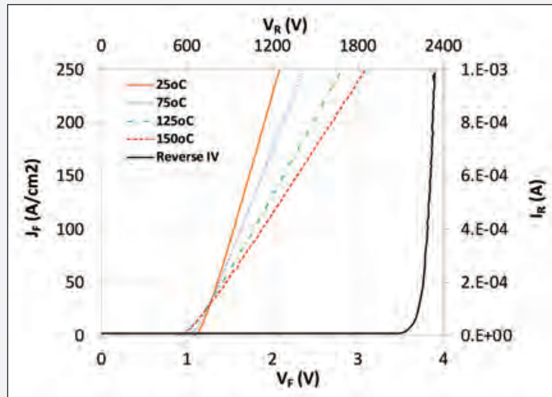


Figure 5. Forward and blocking current-voltage characteristics of a 2 kV SiC charge-balance junction-barrier Schottky diode.

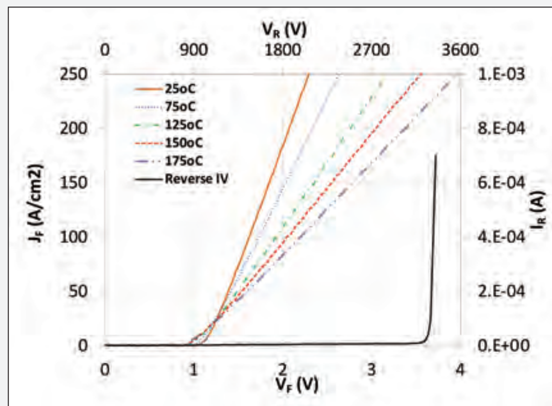


Figure 6. Forward and blocking current-voltage characteristics of 3 kV SiC charge-balance junction-barrier Schottky diodes.

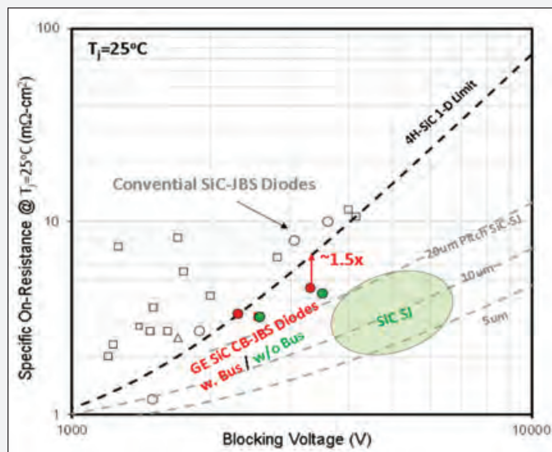


Figure 7. Differential on-resistance versus breakdown voltage for reported SiC FETs and diodes.

cousins have a total of three 10 µm epilayers and two charge-balance regions. Due to these differences, the steps for making 3 kV diodes include the fabrication of an additional charge-balance region, and further epitaxial growth and bus region implantation. In both cases, device fabrication is completed by forming a nickel-based Schottky junction-barrier diode on the top surface, and joining p^+-regions to *p*-connecting regions.

After packaging these devices, we have tested them at both room temperature and elevated temperatures to evaluate their static and dynamic characteristics.

Equipped with a nickel contact, the turn-on voltage for our diodes is around just 1 V (see Figures 5 and 6), while the differential room-temperature on-resistance is as low as 3.5 mΩ-cm^2 and 4.3 mΩ-cm^2 for the 2 kV and 3 kV versions, respectively. These measurements also uncover sharp breakdown voltages at more than 2.3 kV and 3.3 kV. Note that these values are far higher than would be possible with a conventional vertical device architecture sporting a drift layer doped at a concentration of 1 x 10^{16} cm^{-3}.

We have compared the performance of our devices, both with and without connecting regions, to conventional SiC MOSFETs and diodes. Plotting the specific on-resistance as a function of blocking voltage revealed that at more than 3 kV, our devices outperform the theoretical one-dimensional unipolar limit by up to 50 percent, while the level of superiority over commercial devices is even higher (see Figure 7).

Double-pulse switching tests have been used to assess the switching characteristics of our diodes (see Figure 8 for details of the circuit, which features the 2.5 kV/35 A SiC MOSFET, providing an active switch that is capable of turning on and off faster than 100 ns). Traces on an oscilloscope show that during the turn-on of the active switch there is reverse recovery in the charge-balanced junction-barrier Schottky diodes, followed by turn-on of the freewheeling diode during turn-off of the active switch.

These measurements enable us to estimate switching losses from forward recovery and reverse recovery of 12.91 mJ/cm^2 and 1.9 mJ/cm^2, respectively, for the 2 kV devices, and 23.65 mJ/cm^2 and 2.49 mJ/cm^2, respectively, for the 3 kV devices. For nominal conditions of a forward current of 125 A/cm^2, a 50 percent duty cycle, and a

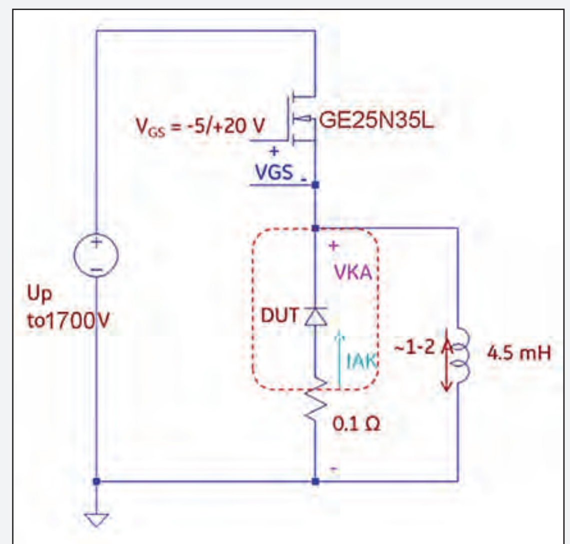


Figure 8. The high-voltage, double-pulse circuit used at General Electric to characterize its SiC charge-balance junction-barrier Schottky diodes assembled in TO-247 moulded packages.

junction temperature of 150 °C, total switching loss for a rated DC-link voltage is approximately 6.2 mJ/cm^2 for the 2 kV device and 12.5 mJ/cm^2 for the 3 kV device. Assuming a thermal limit of 250 W/cm^2, these findings suggest that diodes could operate at frequencies of up to 20 kHz, and thus deliver a disruptive performance in many high-voltage power-conversion applications.

Our results show that SiC Schottky barrier diodes with a novel architecture featuring a charge-balanced drift region can break the one-dimensional limit for on-resistance as a function of breakdown voltage. This success should pave the way to medium-voltage-class SiC unipolar switches with on-state and dynamic losses that are well below those of their silicon counterparts. However, in order to capitalize on these benefits, there needs to be development of disruptive low-inductance and high-voltage packaging and converter topologies with improved thermal performance – and these technologies must accommodate the higher power densities and magnetics associated with the severe changes in voltage and current with time.

We will focus on scaling our developed, charge-balance device drift architecture to higher voltages. This has the potential to disrupt the existing units deployed in many applications that use switching frequencies of less than 1 kHz to more than 10 kHz. Look out for the next device we plan to demonstrate: a 4.5kV SiC charge-balanced MOSFET with a targeted room temperature specific on-resistance of less than 12 mW-cm^2.

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000674 advised by Program Director Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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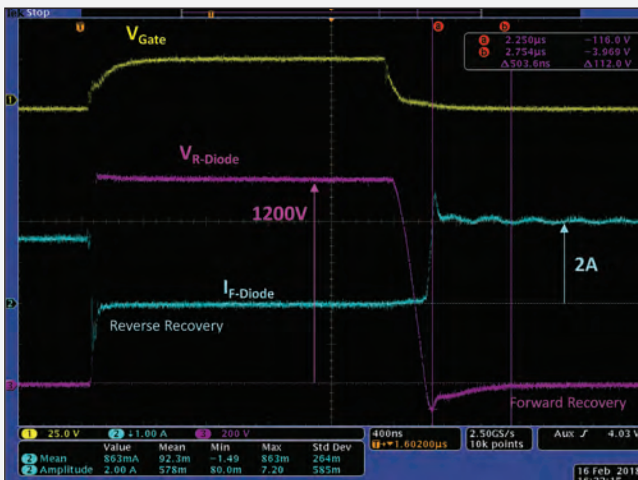

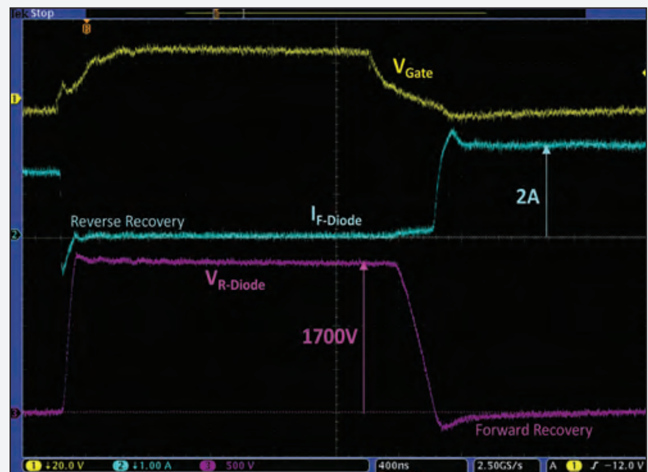

Figure 9. High-voltage double-pulse, diode-clamped inductive switching waveforms using a 2 kV (left) and 3 kV (right) charge-balance junction-barrier Schottky diode as the free-wheeling diode with reverse voltage of either 1200 V or 1700 V and a forward current of 2 A (forward current density is 250 A/cm^2). The yellow trace represents the gate-source voltage of the MOSFET, used to turn-on the active switch and drive the freewheeling diode into reverse recovery until the diode current returns to zero and the load current flows through the switch. The reverse recovery phase of SiC charge-balance junction-barrier Schottky diodes is virtually indistinguishable from those of conventional SiC Schottky diodes. Beyond the reverse recovery phase, the reverse voltage on the charge-balance junction-barrier Schottky diode is 1200 V (left) and 1700 V (right) (these values are about 60 percent of the rated voltage). After some duration, the active switch is turned off and the load current begins to commute to the SiC charge-balance junction-barrier Schottky diode. With the active switch now in the off state, the forward current through the free-wheeling diode quickly ramps from zero to the full load current of 2 A. When turned on from blocking state to conducting state with a fast ramp, the SiC charge-balance junction-barrier Schottky diodes have an observable forward recovery phase. The waveforms show that the forward voltage across the diode has a large peak, before decaying back to nominal value for the forward voltage approximately 500 ns after turn-on. It is believed that this delay is due to the resistance from the p^+ anode to the buried charge-balance regions via the deep *p*-bus regions. This view is consistent with a decrease of one-fifth in turn-on loss at 150 °C.

Addressing production of SiC super-junction MOSFETs

A novel ion-implantation technique improves the manufacture of SiC power devices, including super-junction MOSFETs

BY MICHAEL RUEB FROM MI2-FACTORY

IN THE RUN-UP to the turn of the millennium, a silent revolution took place in the silicon power electronics industry. Back then, the on-resistance of commercial transistors plummeted by a factor of between three and ten, thanks to the introduction of a superjunction architecture in unipolar, high-voltage devices. To create this device, a super-junction is formed by creating *p*-type, high-aspect-ratio columns in *n*-doped vertical drift zones (see Figure 1).

Today, the super-junction is a cornerstone of the silicon power industry. It features in Infineon's CoolMOS, ST-Microelectronics MD-Mesh, Fuji's Super J MOS series, ON Semiconductor's Super FET and Toshiba's DTMOS. This class of devices, which is tending to operate in the 500 V to 900 V range, is serving in switched-mode power supplies in phones, laptops, computers and even server farms. They are a invisible, integral part of our daily lives.

One of the attributes of the super-junction transistor, compared with conventional devices, is a higher doping concentration in the *n*-doped vertical electron conducting path. Blocking capability of the device is maintained by the *p*-columns, which provide local charge compensation, thereby ensuring that the global electric field is low. Thanks to this, super-junction transistors provide an ultra-low ohmic switch with a high blocking capability. That's great from the perspective of a chipmaker, as they can manufacture chips that are smaller – and thus cheaper – for a given on-state resistance. What's more, these chips can fit into smaller packages.

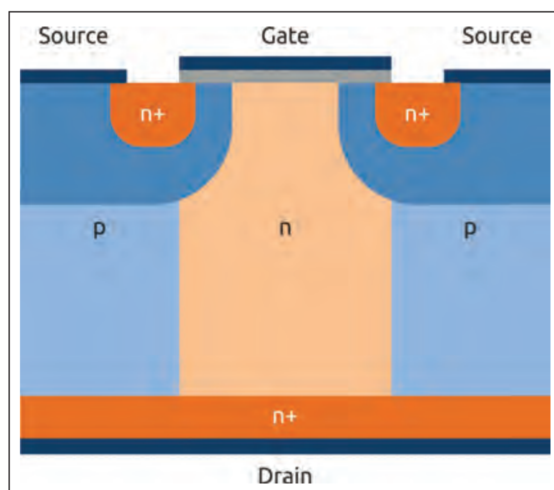

Figure 1. A cross-section of a vertical silicon super-junction device.

Recently, sales of silicon power devices have faced ever-stronger competition from those based on SiC. This rival is setting a new benchmark for the efficiency of high-voltage diodes and transistors, which are being deployed in solar panels, wind turbines and electric cars. However, SiC chips are costly, so they need to improve their bang-per-buck.

Following in silicon's footsteps

A great way to do this is to bring to market SiC super-junction devices. This would lead to a step-change in on-resistance, and propel energy efficiency to a new high, particularly at the highest blocking voltages of 1.7 kV or more. These attributes would allow products to serve in the likes of solid-state transformers and highly efficient energy-transmission systems in high-speed trains.

Note that a related device, the SiC IGBT, is not up to this task: it suffers from a high threshold voltage – it is typically 2.7 V – and bipolar degradation of the material is an issue. Although the latter problem can be overcome, the most common solution so far is a very costly selection of the seed material and a significantly thicker epitaxial layer, leading to additional cost.

SiC super-junction devices also promise to lower the price of this wide bandgap technology, as chips can be smaller, and thus cheaper. Note that as the nominal breakdown voltage rises, the difference in drift-layer

on-resistance between the super-junction design and that of the conventional, unipolar device grows, offering the potential for a greater reduction in chip size (see Figure 2).

Arguably, the biggest challenge associated with the commercialisation of the SiC MOSFET is the development of suitable, high-volume processes for the manufacture of these transistors. It is not possible to simply adopt the techniques used for making silicon superjunction MOSFETs, due to significant differences between the two materials.

For silicon super-junction devices, manufacture tends to involve a multi-epitaxial approach. It begins by ion implanting *p*- and *n*- areas side-by-side in an undoped epitaxial layer to define the *p*-type pillars. Another epi layer is deposited on top, before the implanting process is repeated. Carrying out these steps up to five-to-ten times creates ohmic *p*- and *n*-pillars, which are then subjected to a high-temperature diffusion process (see Figure 3).

With SiC, this approach is not an option. That's because conventional dopants, such as aluminium and nitrogen, have extremely low diffusion coefficients. This means that it is infeasible to diffuse over distances of 3-5 μm, which are required in SiC super-junction designs.

Whatever approach is used has to ensure charge-balancing in the device – and so must realise highly precise doping. That rules out technologies like *p*-doped epi trench filling, because the doping accuracy in the high-volume production of SiC epitaxial layers is rarely better than between +/- 10 percent and +/-20 percent.

The good news is that there is a solution that

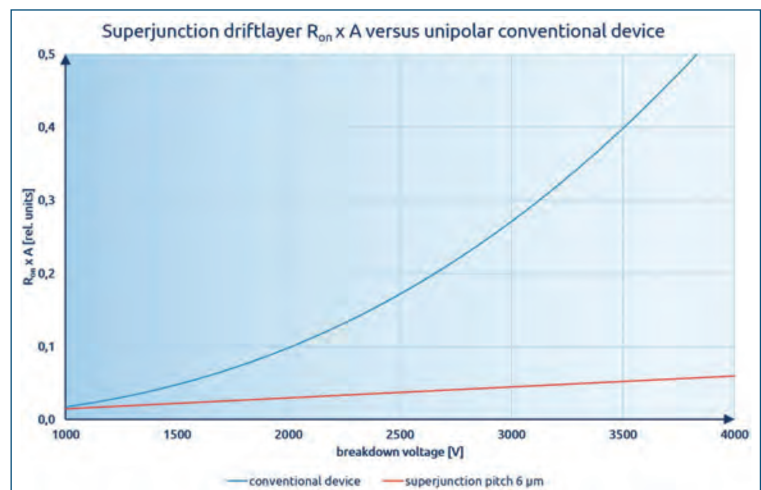

Figure 2. Drift layer on-resistance for conventional and super-junction SiC-power MOS, according to the theory described in Jpn. Patent 9701201.1

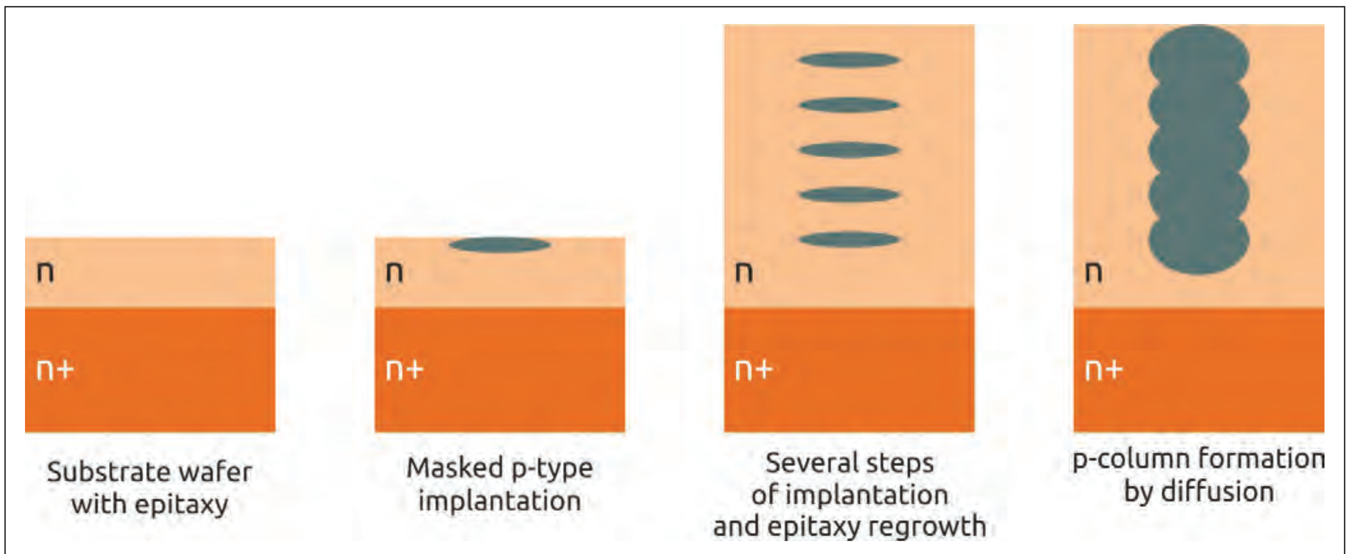

Figure 3. The manufacture of silicon super-junction devices includes a multi-epitaxy manufacturing step.

is applicable to high-volume production: ion implantation, but without diffusion. We are pioneering a form of this at mi2-factory in Jena, Germany. Our technology is capable of producing deep custom-tailored dopant profiles, and while its application to semiconductor manufacturing is new, in a slightly modified flavour it has been successfully applied in heavy-ion cancer therapy for many years.

Our approach differs from the conventional one, whereby monoenergetic ions are 'shot' into a pre-defined depth region known as the projected range. In that case, for a given substrate and ion combination, the projected range is just defined by the ion energy. A single shot creates a gaussian peak of implanted ions. However, it is possible to form extended profiles by creating a sequence of many gaussian profiles, each originating from a different implant energy (see Figure 4).

Unfortunately, extended profiles require many shots.

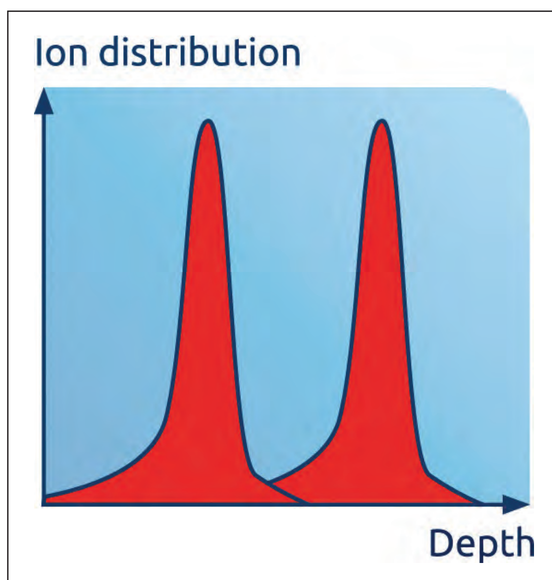

Figure 4. Two ion implantations with different energies result in essentially gaussian peaks.

Simulations suggest that an extended depth range of a few micrometres requires a sequence between 25 and 50 individual implants with differing energies. That's expensive, complicated and error-prone.

We advocate a far simpler approach: one shot, one ion energy and a very special filter. Known as energy filter for ion implantation, our technique involves the use of a micropatterned membrane, which converts a monoenergetic ion beam into a continuum of ion implant energies (see Figure 5). With the membrane in the path, ions are 'shot' not only into one depth, but simultaneously into all depths, where maximum depth is defined by the primary ion energy. With this approach, continuous depth profiles are accomplished in a very straight forward manner (see Figure 6).

Armed with our technology, high-volume manufacture of SiC super-junction transistors is possible. Our approach eliminates the need for diffusion, replacing this with a technique that delivers an extremely high level of precision. Production costs are low – just one step is required for ion implanting, with a process that is capable of both aluminium *p*-type doping and nitrogen *n*-type doping.

One of the primary limitations of our approach is the limited availability of mega-electron ion beams for SiC wafer manufacturing. To address this we offer SiC chip manufacturing customers a loop process option. This serves those in pilot production, and those manufacturing quantities up to medium-volume production – that is, several hundred wafers per month. For higher volumes, we recommend that fabs install industrial tandetron implanters. Further down the line, we plan to refine our technology so that it is compatible with much simpler ion-implantation equipment, rather than just today's industrially applied electrostatic tandetrons.

Although the membranes for our energy filter for

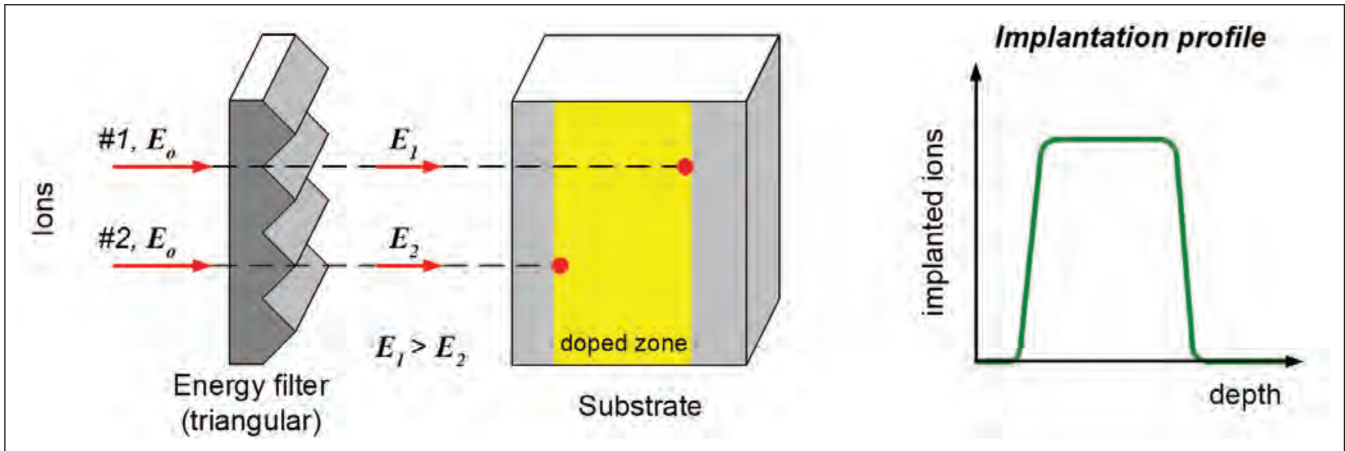

Figure 5. The energy filter for ion implantation pioneered by mi2 factory. The energy of primary ions is modified according to the path length individual ions have to travel through the filter membrane. The long path – through peak – leads to a high loss of energy, while the short path – through a valley – leads to a low loss of energy.

ion-implantation technology are consumables, that does not prevent them from supporting stable, reliable processing. Depending on the ion dose, as many as one hundred 6-inch wafers may be implanted with just a single membrane. Given the very low membrane cost per implant, chip costs generally fall when using our technology, due to benefits that include a reduction in device dimensions associated with the super-junction design.

While our ion-implantation technique may make its case most strongly for the super-junction transistor, it also has a role to play in improving the performance of other SiC power devices, via improvements in doping accuracy (see Figure 7).

For example, 600 V and 1200 V SiC diodes can benefit from our technology. In these devices, the drop in forward voltage is primarily determined by drift layer doping level and thickness – and optimising these two characteristics is governed by the available epi processing technology. For instance, to head off the impact of unintentional low doping levels that result

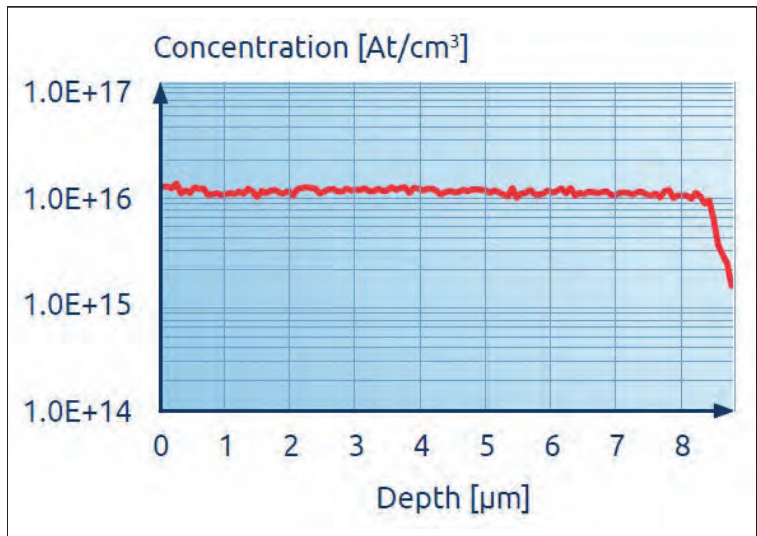

Figure 6. Nitrogen depth profile for 1200 V SiC devices.

SiC Schottky Diodes
- 600V / 650V
- 1200V
- (1700V)

Shrink and Yield

SiC SJ MOSFET

> 3300V

Shrink and Yield

Si IGBT
- n-doping
- lifetime-management

Performance

Figure 7. The energy filter for ion-implantation technology developed by mi2 factory can be used for making diodes and transistors.

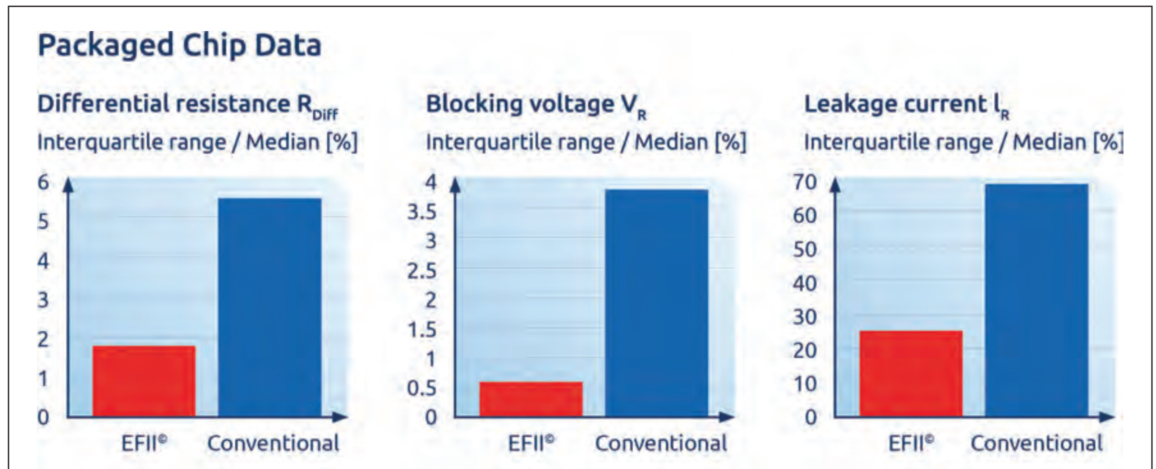

Figure 8. Results from an early R&D project with a chipmaking industrial partner highlight the reduction in the spread of key attributes for diodes.

from process variations, SiC diodes are generally designed larger than they would be if optimum processing conditions were available. By switching from *in-situ* doping during epi deposition to our superior energy filter for ion-implantation technology, we estimate that it may be possible to shrink the area of the 1200 V device by about 20 percent.

This claim for a reduced chip size is supported by work that we carried out several years ago. Back in 2014, in collaboration with an industry partner, we took part in an R&D project to investigate the impact of doping precision. During this programme, we compared the variations in key characteristics of 600 V merged *p-i-n* Schottky diodes from regular production with those formed with our ion-implantation technology. We found far narrower parameter distributions for differential resistance, blocking voltage and leakage current, highlighting the potential of our energy filter for ion-implantation technology to reduce chip sizes (see Figure 8).

Today, our technology is well-placed to provide the essentially homogenous doping profiles that are needed for diodes and super-junctions. In future, the design of these devices is tipped to evolve, with the introduction of graded drift-layer doping profiles that will propel efficiency to a new level. We intend to support this, having just started to develop an advanced form of our technology that will be capable of delivering more complex doping profiles.

To support this work, and ultimately our customers, we have developed a software tool that is capable of simulating all types of filter-substrate constellation. This includes masked substrates (see Figure 9). We are confident that interest in our technology will grow. The SiC super-junction is destined to deliver a hike in power-transistor efficiency, and our energy filter for ion-implantation technology is a key enabling technology for the production of these devices. Other diodes and transistors will also benefit from our approach to doping, with the greater accuracy provided by our technology enabling a trimming of dimensions, leading to significant cost savings.

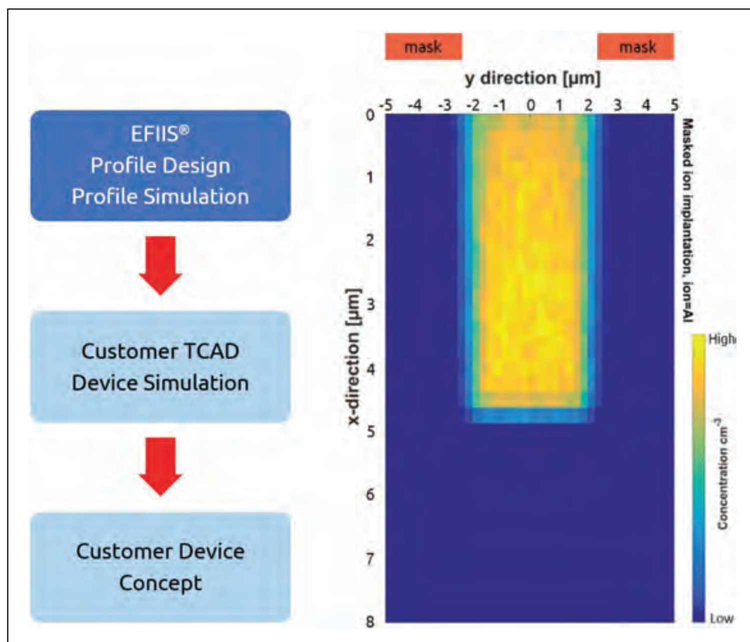

Figure 9. Left: The approach that mi2 factory takes for supporting customer device design with its energy filter for ion-implantation. Right: A 5 µm-deep *p*-column created in SiC using an energy filter for ion-implantation.

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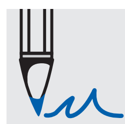
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Superior silicon carbide

Solution growth eliminates basal plane dislocations in high-quality single crystals of bulk SiC

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THE GLOBAL DEMAND for electricity is rising far faster than that for all forms of energy. According to the International Energy Agency, worldwide energy demand increased by 2.1 percent in 2017, while that for electricity climbed by 3.1 percent.

As electricity usage rises, the total gains resulting from more efficient power devices will become ever more significant. This makes it more attractive than ever for humanity to invest in SiC diodes and transistors, which have much lower losses than their silicon siblings.

Right now, sales of SiC devices are climbing fast. But even more success is possible, along with a greater share of the power semiconductor market, if SiC manufacture were to include the production of substrates that are cheaper, larger, and exhibit a higher crystal quality. Read on to discover how this can be accomplished.

Growing single crystals of SiC is far from easy. The 4H-SiC single crystal substrates that are on the market today are plagued by various dislocations – in total, the density of imperfections is in the range of thousands to ten thousand per cm^2 (see Table 1 for a list of common dislocations, and Figure 1 for an illustration of how they may appear in 4H-SiC single-crystal substrates). These dislocations are a menace, driving down device manufacturing yield and applying the breaks to far greater deployment of SiC power devices.

By far the most troublesome class of dislocations are the line defects in the 4H-SiC{0001} basal planes. Known as basal plane dislocations, these killer defects wreak havoc with device performance. It drops when a forward voltage is applied across 4H SiC MOSFETs and *p-i-n* diodes, and basal plane dislocations are driven from the SiC single-crystal substrates to the epitaxial layers, where they expand and turn into Shockley-type stacking faults. There they act as high-resistance layers, increasing the on-state voltage and driving a deterioration in device performance.

One way to address this issue is to convert the basal plane dislocations into threading-edge dislocations at the interface between the epitaxial stack and the substrate. This conversion must take place during the epitaxial growth, by CVD, of layers on the SiC substrate. Note that the threading-edge dislocations that are formed are harmless, as they don't degrade

Types of Dislocations	Direction of dislocation	Burgers Vectors	Density (cm^{-2})
			Commercially available wafer
Threading Screw Dislocation (TSD)	// c-axis	n<0001> (n=1, 2)	500-3000
Threading Edge Dislocation (TED)	// c-axis	1/3<11-20>	3000-10000
Basal Pane Dislocation(BPD)	⊥ c-axis	1/3<11-20>	500-7000

Table 1. Types and density of dislocations in 4H-SiC crystals

device characteristics. However, as it is not possible to convert every single basal plane dislocation into a threading-edge dislocation, this is an imperfect solution. It would be far better to completely eliminate the basal plane dislocations in SiC.

Unfortunately, it is challenging to produce SiC crystals, the starting point for substrate production. At normal pressure, there is no liquid phase of SiC with a chemical composition for the melt that matches that of the solid state. Consequently, it is theoretically impossible to carry out melt growth by solidification, which is the approach adopted for making silicon boules.

Due to this limitation, today's SiC substrates are manufactured with a gas phase method that can produce 4H-SiC bulk single crystals. Sublimation takes place at temperatures of at least 2,300 °C. Stresses associated with the high temperatures, and cooling down from them, give rise to thermal stress. This is released by movement in 4H-SiC basal planes, which are easy slip planes, and results in basal plane dislocations with a density of hundreds per cm^2 or more.

The highest quality crystals formed by the sublimation method are those that have been made by a team from Toyota Central R&D Labs, Japan, using repeated *a*-face (RAF) growth. However, this material is not free from basal plane dislocations.

To eradicate these dislocations, an alternative growth method is required. That's the approach that our team from Nippon Steel and Sumitomo Metal Corporation and Toyota Motor Corporation is taking, using a solution growth technique to realise ultra-high-quality SiC single crystals.

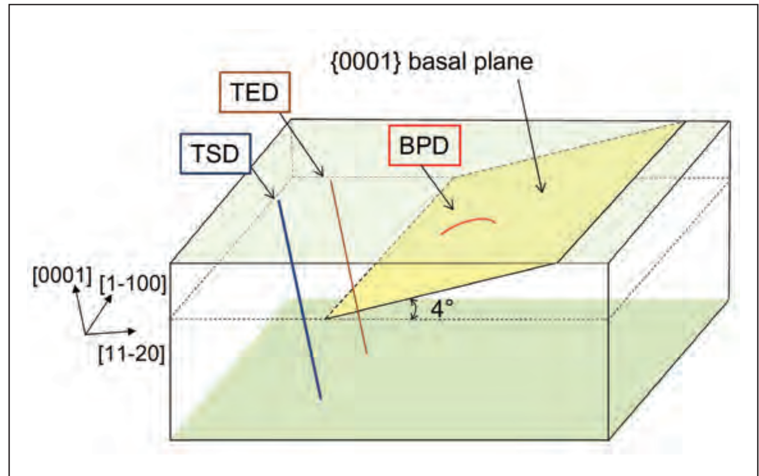

Figure 1. Dislocations in a 4H-SiC single crystal substrate (4° off-axis)

Our approach is a form of liquid phase growth. SiC is dissolved in a metallic melt that contains chromium or titanium, with supersaturation driving the formation of the crystal. With this approach, the reaction takes place at close to the thermodynamic equilibrium state, enabling the crystal growth to proceed at a temperature that is lower, by a few hundred degrees Celsius, than it would be for a sublimation method (see Figure 2).

Suppressing solvent inclusions

One of the challenges with our approach is that as the SiC crystal forms from a liquid phase, we must prevent the surface from roughening as the material thickens. This threat, known as surface morphology instability, can create concavities and convexities with dimensions of several hundred microns to several millimetres. In the fine concavities, any solvent microdrops that are left can spawn macroscopic defects, known as solvent inclusion.

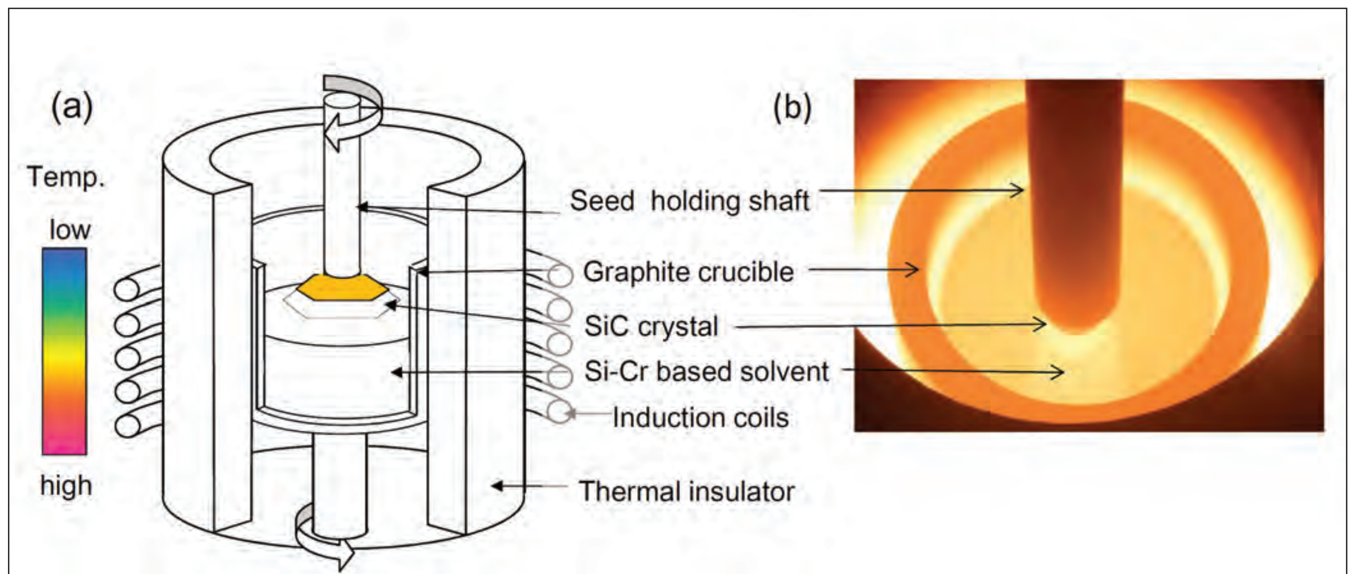

Figure 2. (a) The SiC solution growth set-up used by engineers at Nippon Steel and Sumitomo Metal Corporation and Toyota Motor Corporation. The graphite crucible, which provides a container for the solvent and a carbon source, is directly heated by induction. Growth, typically at 2000°C, is conducted under atmospheric pressure in a mixture of helium and nitrogen gases. (b) Inside a crystal growth furnace.

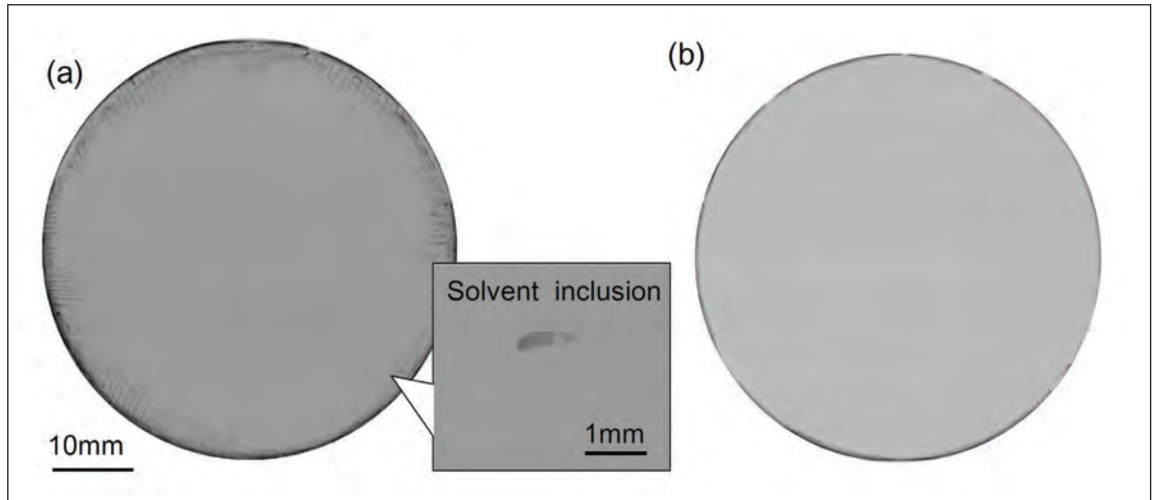

Figure 3. Transmission X-ray images of 2-inch-diameter 4H-SiC ingots (a) before optimising crystal growth conditions, and (b) after optimisation. It is clear that several dark domains exist at the peripheral part on the crystal, formed using the conventional growth technique. These domains are ascribed to a metal solvent that has a lower X-ray transmittance compared with the SiC matrix. Note that no dark domains are observed for the whole volume in the crystal after optimising growth conditions, indicating that this material is free from solvent inclusion.

Substrates with this form of imperfection are unsuitable for making power devices. So, to prevent them forming, the growing surface has to be smooth for extended periods of time during crystal growth. That's a very demanding technical challenge that has remained elusive for many years.

We have overcome this challenge by considering the numerous process factors associated with crystal growth. Taking this approach reveals that it is possible to stabilise the surface morphology, and ensure a smooth surface, by controlling the growing interface outline while suppressing changes in supersaturation over time. By adopting these findings, we have produced the first 2-inch bulk crystals that are free from solvent inclusion (see Figure 3).

Using the solution growth method, we have also

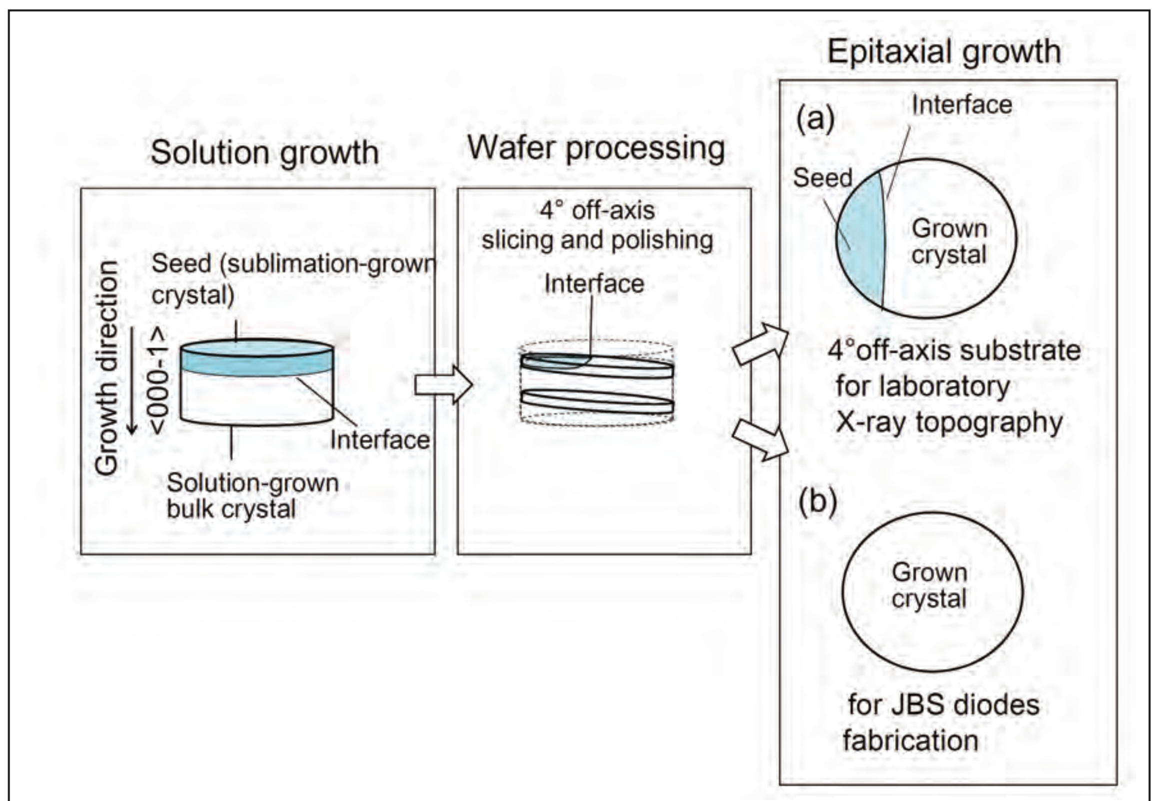

Figure 4. Slicing the material produced by the solution growth method creates (a) wafers for evaluating dislocations, and (b) wafers for prototyping junction barrier Schottky diodes.

produced 4-inch crystals that are more than 10 mm-thick. An obvious next step is to apply the solvent inclusion elimination technology that we have established for 2-inch diameter crystals to the growth of those that are 4-inch in diameter.

Those of us at Nippon Steel and Sumitomo Metal Corporation are drawing on this growth technology to produce, from ingots, 2-inch diameter 4H-SiC substrates with an off-angle of 4°. These can provide a great foundation for making for power devices.

To evaluate the quality of our SiC substrates, we have compared the dislocation density of our crystals produced by the solution growth method – from now on referred to as solution-grown crystals – with that of a seed crystal. This has been accomplished by using the solution growth method to grow a crystal on the on-axis plane ($000\bar{1}$) of a seed crystal. Tilting this at 4°, and slicing and polishing wafers from it, creates a sample that includes the interface between the seed crystal and solution-grown crystal.

We deposited a 10 μm-thick layer on this sample by CVD, before scrutinising the material with X-ray topography (see Figure 4). This reveals that the seed crystal area features a high-density mesh contrast, originating from basal plane dislocations. Meanwhile, in the solution-grown crystal area, no such contrast is observed.

These findings indicate that there are no basal plane dislocations in the solution-grown crystal (see Figure 5). In addition, they show that when the basal plane dislocations in a seed crystal in the {0001} plane intersect at right angles with the crystal growth direction, they do not propagate into the solution-grown crystal. Yet another insight provided by X-ray topography is that the solution growth and cooling processes do not generate any new basal plane dislocations. We attribute this to the lower temperature for solution growth than for sublimation growth.

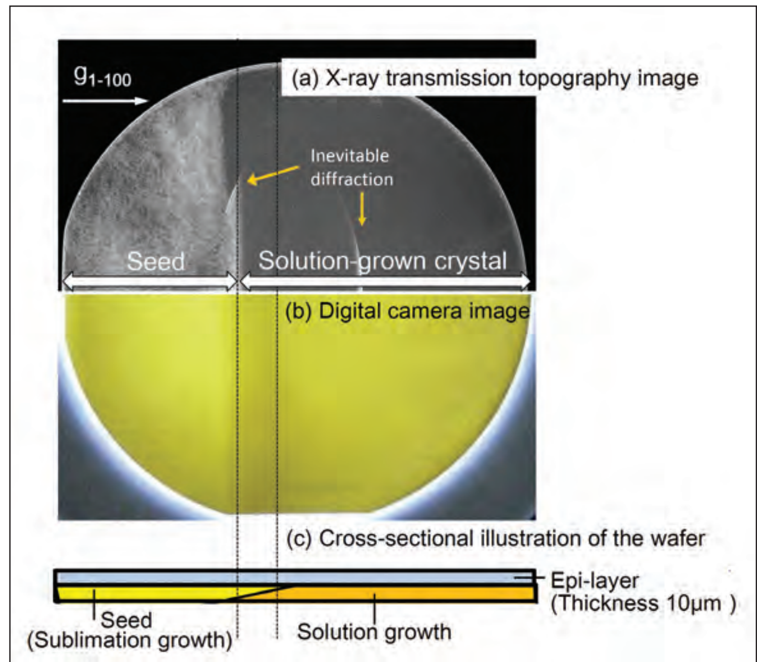

Figure 5. 2-inch diameter 4H-SiC wafers have been analysed by (a) transmission X-ray topography, (b) digital camera images, and (c) by taking cross-sections.

To ensure high-performance devices, the surface of SiC must be impeccably clean. This includes incredibly low levels for metallic contaminants on the surface, as their presence can degrade the characteristics of a power device, and compromise yield.

As our solution growth involves a chromic solvent, there is a danger that this might impair the quality of our material. To see if that is the case, we have quantified the metallic impurities on the front and back sides of our of epitaxial wafers, using inductively

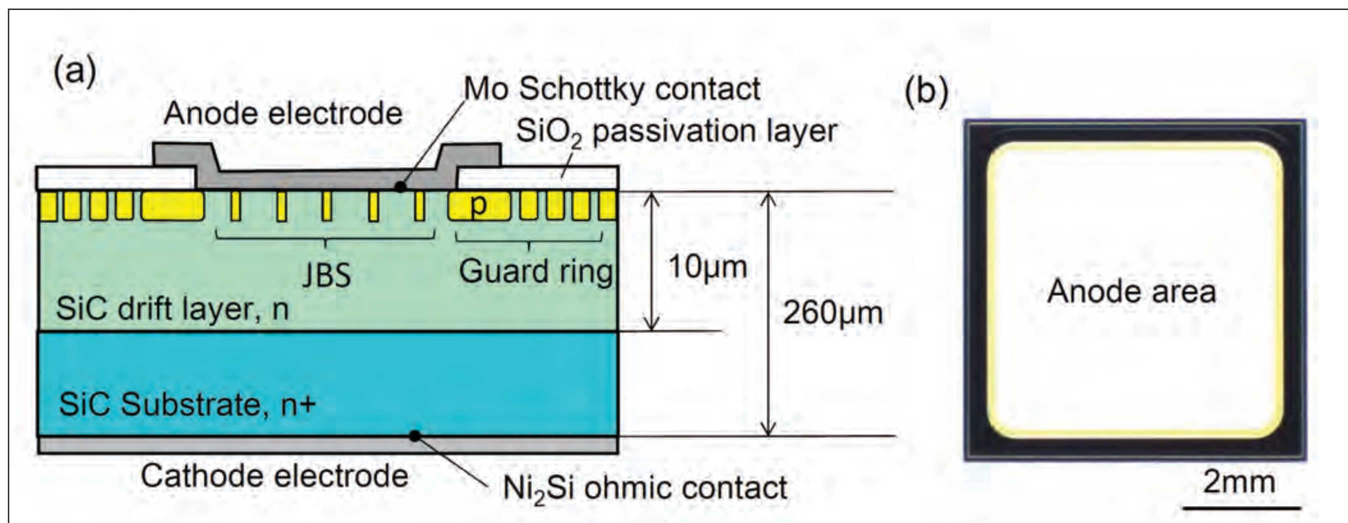

Figure 6. (a) A vertical cross-sectional view of junction barrier Schottky diode. (Taken from H. Fujiwara *et al*. Appl. Phys. Lett. **100** 242102 (2012). (b) Plan view of a junction barrier Schottky diode. Active area is 6 mm by 6 mm.

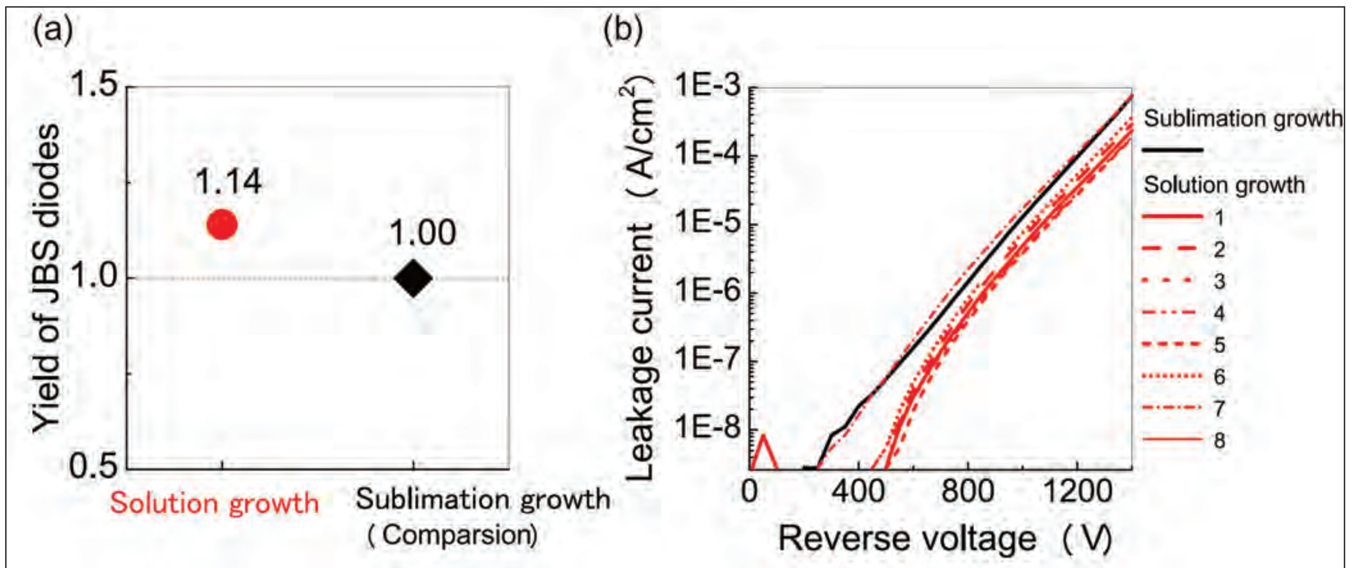

Figure 7. (a) A comparison of the proportion of efficient junction-barrier Schottky diodes fabricated on solution-grown and sublimation-grown SiC substrates. Note that the yield of the junction-barrier Schottky diodes fabricated on the solution growth substrate was normalized by that obtained on the sublimation-grown substrate. (b) Relationship between reverse current and voltage characteristics for the junction barrier Schottky diode.

coupled plasma mass spectrometry and direct acid droplet decomposition.

This technique reveals that the front and back sides of our wafers have negligible levels for many common metals – values were below 3.5×10^{11} atoms/cm^2 for more than a dozen common elements: calcium, sodium, potassium, magnesium, titanium, chromium, manganese, iron, cobalt, nickel, copper, zinc and aluminium. We believe that the extreme cleanliness of the surfaces of our solution-grown SiC wafers could result from the availability of bulk crystals without solvent inclusion. Such low levels of contaminants confirm that there are no concerns associated with using solution-grown SiC epitaxial wafers in device manufacturing lines.

Building better devices

We have fabricated the world's first junction-barrier Schottky diodes at the wafer level on solution-grown SiC. For the production of these devices, we used a 2-inch diameter solution-grown 4H-SiC substrate (see Figure 6).

To evaluate the electrical performance of the diodes, we compared their performance with equivalents grown on commercially available, high-grade substrates manufactured by sublimation. The efficiency and electric characteristics of devices grown on our substrates are equal to, or higher than, those grown on the alternative foundation (see Figure 7).

This test is not ideal for highlighting the superiority of our substrates. That's because basal plane dislocations in the substrate have little effect on the degradation of electric characteristics of a junction barrier Schottky diode. Where our substrates promise to make a far bigger contribution is to improving the performance of diode-built-in MOSFETs and 4H-SiC *p-i-n* diodes. When prototypes of these devices are made on our substrates, they will demonstrate the overwhelming superiority of solution-grown SiC crystals.

We have made much progress, but there is still work to do. Today, sublimation is used for high-volume manufacture of 6-inch diameter SiC, while the diameter of solution-grown wafers is still small, delaying success in the marketplace.

However, when solution grown SiC material hits the market, success could be rapid. This form of substrate will be in much demand, thanks to its absence of basal plane dislocations, a known killer defect that is an obstacle to obtaining high-performance, highly-reliable SiC power devices. What's more, for this form of substrate, costs have the potential to fall below those made by sublimation, as growth takes place at normal pressure and under lower temperatures.

Further reading

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Rohm braves high voltage SiC markets

With its 1700 V SiC power module delivered, Rohm is eyeing even higher voltage markets and industry domination, reports Rebecca Pool

BE IT FOR PHOTOVOLTAICS, electric vehicles, 5G infrastructure or industrial high-power supplies, SiC is steadily infiltrating markets around the globe. As analysts forecast a compound annual growth rate of at least 25 percent, and a $1.5 billion SiC market come 2023, industry players up and down the supply chain are readying for action.

US-based GT Advanced Technologies recently opened a SiC crystal growth facility to meet the imminent SiC market boom while Infineon has bought SiC wafer-splitting process developer, Silectra, to secure substrate supply.

Wolfspeed, Infineon, GeneSiC and more are diligently pioneering packaging structures to take on the extreme switching speeds and temperatures that SiC can handle. And in a bold move, Cree has sold its Lighting business to focus on power semiconductors, having spent the last year-and-a-half year bolstering its SiC supply and honing devices.

Amongst these front-runners is Japan-based Rohm, having had its eyes firmly fixed on SiC for some two decades. Preliminary SiC MOSFET development began in 2002, with initial samples shipped in 2005. Trial manufacture of 300 A MOSFETs followed in 2007 with trench-type devices released in 2008.

Then, in 2009, the company acquired SiC crystal manufacturer, SiCrystal, with the now vertically integrated business delivering its first mass-produced SiC Schottky diodes and MOSFETs in 2010. Mass-produced full SiC modules followed in 2012 with Schottky barrier diodes on 6-inch wafers delivered in 2017.

Today, the company claims to have the industry's largest line-up of automotive-grade 650 V and 1200 V SiC MOSFETs, but is also intent on delivering devices at ever-higher voltages for more and more gruelling applications. As Aly Mashaly, Power Systems Manager at Rohm highlights, the industry trend towards higher power density has led to higher systems voltages. And, given this, the company recently developed a 1700 V, 250 A rated SiC power module that is currently being used in customer projects.

According to Mashaly, the module's high voltage surpasses the requirements of electric hybrid vehicles, for now, but is instrumental in inverted and converter applications for outdoor power-generation systems and industrial high-power supplies.

Crucially, the latest system promises to provide the same energy-saving performance as 1200 V devices with a high reliability, meaning the 1700 V SiC module is ready to take on the 1700 V silicon IGBT module.

"The big challenge in silicon carbide is to provide high reliability, especially at higher voltages," says Mashaly. "But we have tested our devices at high voltages, temperatures up to 85 °C and high humidities, and for more than 1000 hours, and we haven't seen any degradation in performance."

The module comprises SiC MOSFETs and Schottky barrier diodes, vastly diminishing chip area and reducing on-resistance by 10 percent relative to similar SiC products, says Mashaly. But while this cuts energy use and heat dissipation, it doesn't cut upfront costs, a fact that the Power Systems Manager knows only too well.

"We are working to reduce the level of the price compared to the IGBT [module], and while I cannot provide exact numbers, I do know that we will always be getting closer," he says. "I don't ever expect the cost of the SiC module to come down to that of the IGBT module but if we look at system cost , the benefits of using SiC has already been proven to many tier one companies and automotive OEMs."

So with the demand for SiC power devices rising, how exactly is Rohm meeting market needs? While

the company is in the process of ongoing capacity expansion at its Nuremberg site, in June 2018 it revealed plans to massively expand SiC production capacity at its Apollo plant in Chikugo, Japan. Construction has now started and will continue until at least the end of 2020.

At the same time, the transfer of manufacturing from 4-inch to 6-inch wafers is also well underway, boosting production efficiencies. “We have already started this for our planar MOSFETs and this year we will try to make this transition with our trench MOSFETs,” says Mashaly.

What’s more, Mashaly reckons that the wafer quality of Rohm’s 6-inch wafers is better than that of its 4-inch wafers. “We have nineteen years of experience in SiC and we saw a huge improvement in the quality of [our] four-inch wafers compared to two-inch wafers, and we now see that quality is even better with the six-inch wafers,” he says. “Year by year we have this improvement in our production process and we are confident that the quality in the next level of substrate will be high.”

So with manufacturing in hand, where next for Rohm on the road to SiC success in an increasingly crowded market-place? Mashaly is keen to highlight that aside from Wolfspeed, Rohm is the only vertically integrated business in this market, and as such, intends to capture 30 percent market-share by 2025, making it the number one player.

And as well as an ever-larger market share, the company will also be looking towards ever-higher voltages. “Right now we are focusing on the 1200 V and 1700 V areas due to the big potential for mass production of SiC here,” he says. “But we already have research and development activities in place for 3.3 and 6.5 kV [devices]... we don’t have a defined time when we will launch these products but we also see the potential for SiC here.”

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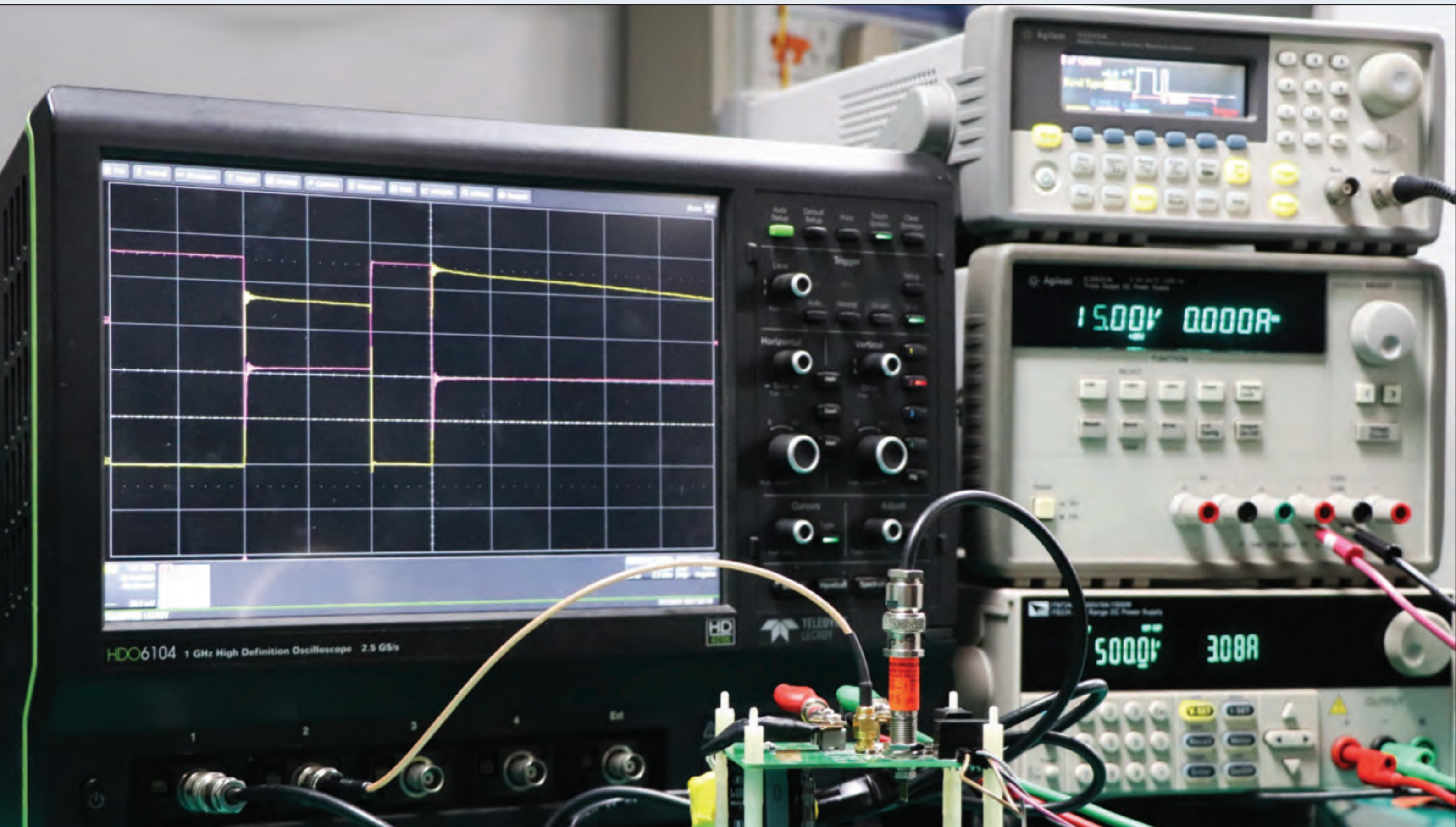


Obliterating dynamic on-resistance degradation

Vertical GaN-on-GaN power devices enable current-collapse-free performance

BY SHU YANG AND SHAOWEN HAN FROM ZHEJIANG UNIVERSITY

GaN IS DESTINED to revolutionise the power electronics industry. Devices that are made from this material can operate at high frequencies while offering low conduction and switching losses – attributes that allow the production of electrical units that combine enhanced energy efficiency with increased power density and a reduction in the size and weight of the system. It is these strengths that enable a hike in the performance of smartphone and laptop chargers, photovoltaic inverters, power supplies for data centres, on-board chargers and charging stations for electric vehicles and hybrids.

The most common form of this class of device is the GaN-on-silicon transistor. It has come on in leaps and bounds over the last decade, and is now driving the commercialisation of this technology.

One of the merits of GaN-on-silicon is the low cost of 150 mm and 200 mm silicon substrates.

But that's not the only reason behind low-cost production: the epiwafers can be processed in fully-depreciated 150 mm and 200 mm silicon fabrication lines.

These GaN-on-silicon devices, however, are usually confronted with a challenge that could cause excess power loss, known as either dynamic on-resistance degradation or current collapse.

Recently, our team at Zhejiang University in China has shown that it is possible to overcome this issue by turning to GaN-on-GaN devices with a vertical architecture and nitridation-based termination.

Trapping issues in GaN-on-silicon

To block high voltages, conventional lateral power devices comprise of a semi-insulating III-nitride buffer stack, located between the GaN channel layer and the silicon substrate. This buffer stack tends to contain a high density of bulk traps, some of which originate from crystalline defects and dislocations due to the lattice and thermal expansion coefficient mismatch between the nitride layers and silicon.

There are also deep-level acceptor traps, resulting from carbon atoms sitting on nitrogen sites. During the growth of epilayers, carbon is intentionally/unintentionally incorporated to compensate for donor-type background impurities, such as silicon and oxygen. This enables the buffer stack to exhibit a high resistivity with a low leakage.

In these lateral devices, the high-density two-dimensional electron gas, which features a high electron mobility, equips the transistor with a low static on-resistance. But when this device is switched from a high-voltage off-state, excess power loss results, due to the ailment known as either current collapse, or an increase in dynamic on-resistance.

Several factors contribute to this degradation (see Figure 1). When this lateral device is operated in its off-state with a high drain bias, the large negative gate-to-drain bias can lead to electron injection and trapping at the polarized III-nitride surface in the gate-to-drain access region. Meanwhile, in the vertical direction, the large positive drain-to-substrate voltage could cause electrons to be injected from the silicon substrate and trapped in the GaN buffer stack.

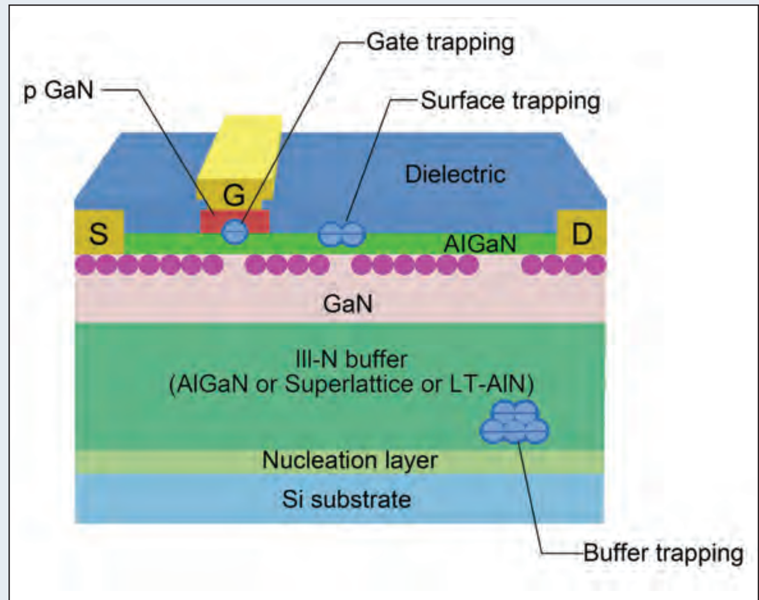


Figure 1. An illustration of trapping-induced current collapse, using a *p*-GaN HEMT as an example.

Another issue is that when this device is running in a high power state, a hard-switching transition can generate hot electrons in the channel. From here, these electrons may then be injected and trapped at either the III-nitride surface or the III-nitride buffer stack. When switching the device on, it may take considerable time to release electrons from surface states and buffer traps. If this happens, the two-dimensional electron gas in the gate-to-drain access region could remain partially depleted, resulting in current collapse and conduction loss.

A third factor at play is that when a lateral *p*-GaN HEMT or insulated-gate GaN power transistor is operated in its on-state with a gate overdrive, trapping

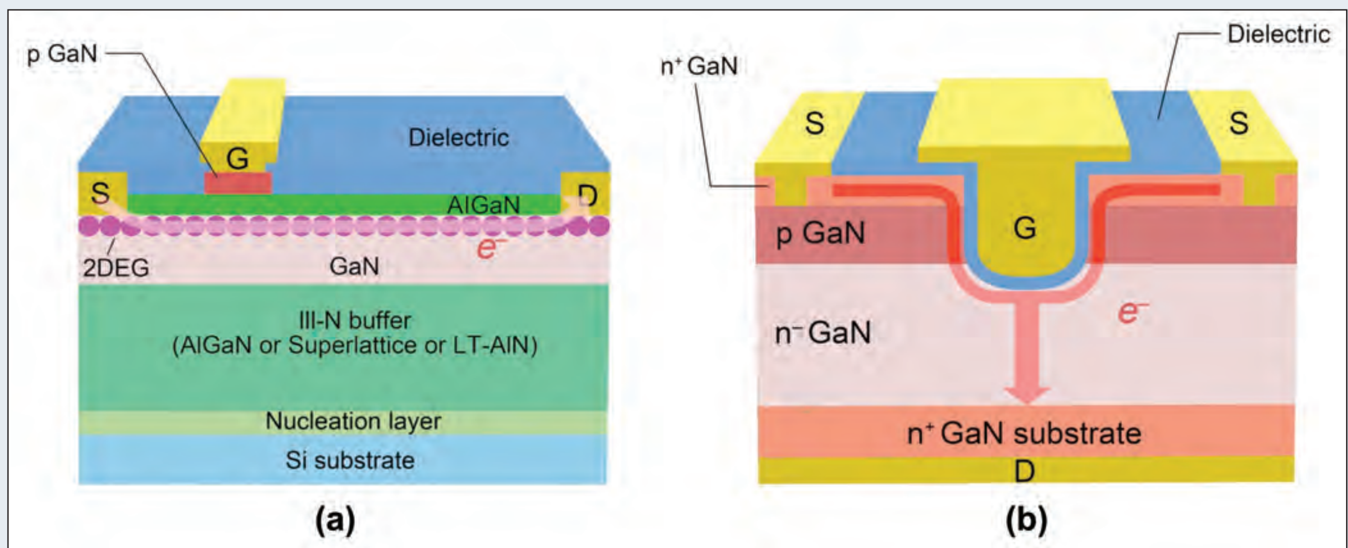


Figure 2. Schematic cross sections of (a) lateral GaN-on-silicon and (b) vertical GaN-on-GaN power devices showing different electron flows.

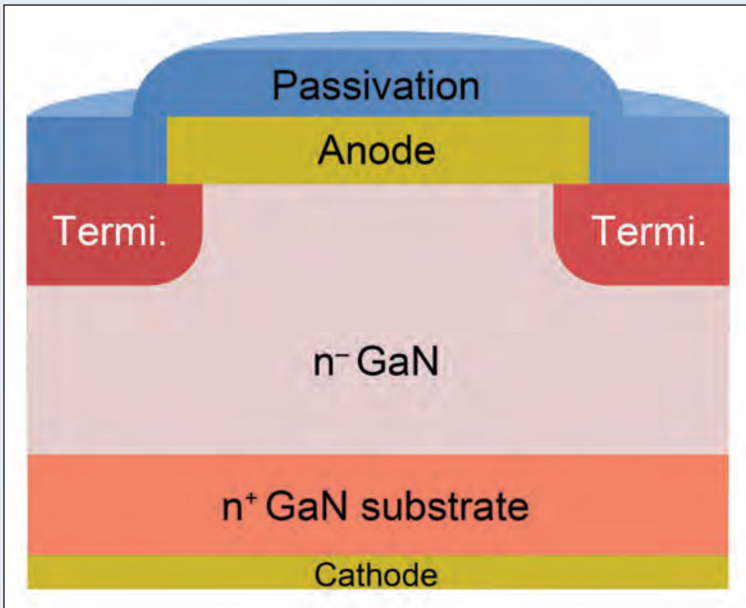


Figure 3. Researchers at Zhejiang University, China, have developed the vertical GaN-on-GaN Schottky barrier diode with nitridation-based termination.

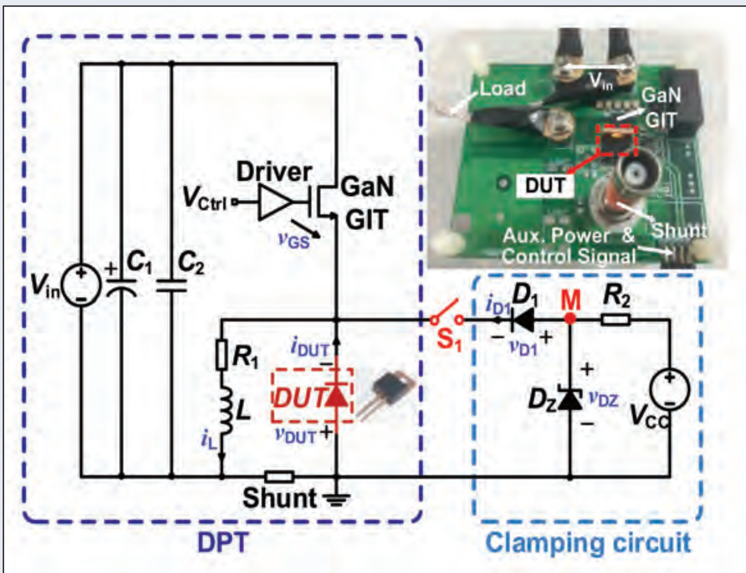


Figure 4. The team at Zhejiang University has developed a high-speed double pulse tester with a clamping circuit to provide quantitative, precise extraction of dynamic on-resistance, R_{ON}, in GaN devices.

can occur in the interface and border region beneath the gate electrode. A positive shift in threshold voltage could result, creating a reduced gate overdrive at a pre-set on-state gate bias and an increase in the on-resistance.

To combat all these issues, researchers have developed multiple field plates, advanced dielectric passivation, buffer stack optimization and hybrid drain techniques for mitigating trapping effects. Despite the effectiveness of these approaches to some extent, it's relatively difficult to completely eliminate the root cause for trapping effects, and current collapse is still regarded as one of the biggest challenges for lateral GaN-on-silicon power devices.

From lateral to vertical

The recent emergence of high-quality, free-standing GaN substrates has opened the door to the development of vertical GaN-on-GaN power devices. Merits of growth on a native substrate include the elimination of lattice- and thermal-mismatch between the epitaxial layer and the substrate, making it possible to produce thicker GaN drift layers with a lower dislocation density. This architecture also trims thermal resistance, thanks to the removal of a thermal boundary resistance in the nucleation layer between the III-nitride buffer and the silicon substrate (see Figure 2). Armed with all these attributes, the vertical GaN-on-GaN power devices can deliver high current capacity, a high breakdown voltage, more efficient chip area utilization, and superior thermal performance.

A significant challenge for high-voltage vertical power devices is to address electric field crowding at the junction edge. Left unchecked, this crowding can result in excess reverse leakage and premature breakdown. The conventional approach to suppressing edge-effect-induced reverse leakage and enhancing breakdown voltage is to apply edge termination techniques. However, in GaN devices, it is not easy to implement junction-based edge termination techniques, such as junction termination extension and field-limiting rings, due to the low-efficiency of selective *p*-type doping and activation.

To address this issue, we have recently developed a nitridation-based termination technique that is well suited to vertical GaN devices (see Figure 3). We form the nitridation-based termination structure by applying a low-damage nitrogen plasma treatment to the periphery of the device area with an optimal RF power and time.

According to experiment, this approach shifts the Fermi-level in the nitridation-based termination region towards the valence band. This shift is most likely to result from a favourable modification of the surface conditions, such as the enhanced adsorption of nitrogen atoms and passivation of gallium dangling bonds.

One of the benefits of applying nitridation-based termination around the device periphery is that it produces an enlarged energy barrier height and/or effective barrier thickness at the junction edge. In turn, this suppresses electron transport via thermionic field emission or tunnelling, and ultimately slashes reverse leakage by four orders of magnitude while enhancing breakdown voltage – the later increases to around

All of these tests demonstrate that our vertical GaN-on-GaN power rectifier is free from dynamic on-resistance degradation just 200 ns after switching from a high-voltage off-state, outperforming the state-of-the-art lateral GaN-on-silicon devices

1 kV. In addition to these benefits, our vertical GaN-on-GaN diode exhibits a nearly ideal Schottky contact, an on-resistance of 1.2 mΩ·cm², and an on/off current ratio of 13 orders of magnitude.

Testing challenges

There are a lack of reports providing quantitative, systematic characterisation of the dynamic on-resistance of vertical GaN devices. To gain insight into the dynamic on-resistance, some researchers have undertaken on-wafer pulsed current-voltage measurements. However, such wafer-level test tends to exhibit a relatively long measurement delay, due to parasitics in the commutation loop. This delay allows time-dependent recovery – or de-trapping – to occur, threatening an underestimation of the trapping effects, alongside inaccurate evaluation of the dynamic on-resistance.

One way to overcome this limitation is to use a custom-designed board-level test that is capable of capturing fast transients on a sub-microsecond timescale. Note that an accurate assessment of the dynamic on-resistance on a timescale of hundreds of nanoseconds is of particular interest and importance to GaN devices, as they are expected to switch at frequencies of more than a megahertz.

We have developed a double pulse test circuit with an optimized layout and minimised parasitics to obtain an accurate assessment of the dynamic on-resistance (see Figure 4). In this set-up, the device under test, the vertical GaN Schottky barrier diode, acts as a freewheeling diode, while a commercial 600 V, GaN HEMT serves as the control switch.

This configuration provides an accurate, precise extraction of dynamic on-resistance. Thanks to the diode-based clamping circuit, a precise measurement of the low on-state voltage after switching from a high-voltage off-state can be provided. Because of the ultrashort delay of 200 ns in the high-speed test board, the possible trap recovery during measurement can be minimised such that dynamic on-resistance can be accurately extracted.

To evaluate the benefit of our device, we wish to compare its performance to that of a state-of-the-art lateral GaN-on-silicon device. A commercial, lateral GaN-on-silicon diode is not currently available. But we can make a comparison with state-of-the-art E-mode GaN-on-silicon transistors, by electrically shorting the gate and source terminals. With this modification – enabling the transistor to operate as a power diode when operating in the reverse conduction mode –

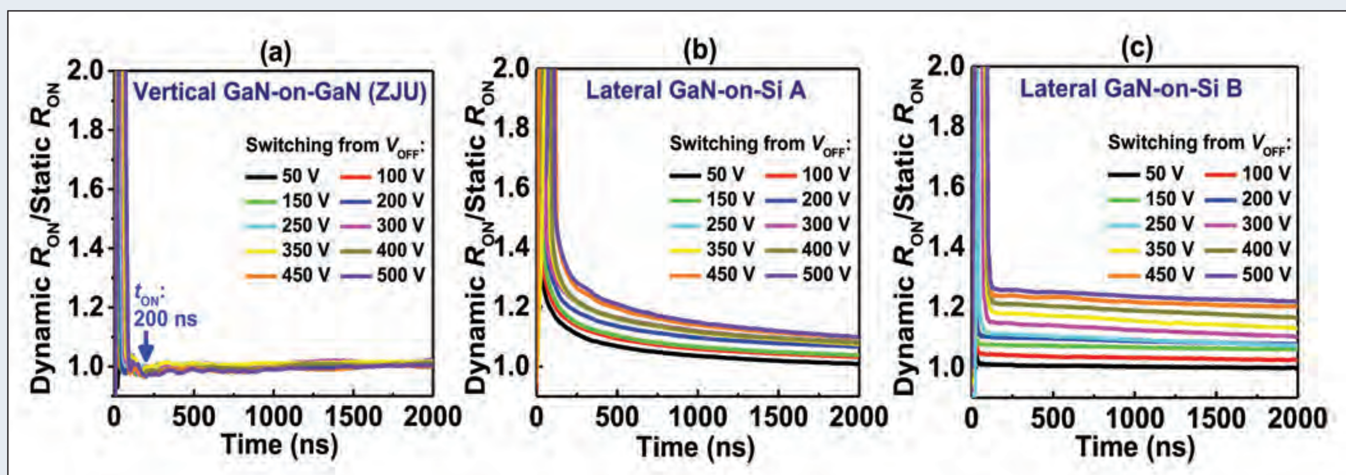


Figure 5. Time-resolved dynamic R_{ON}/static R_{ON} of: (a) a vertical GaN-on-GaN Schottky barrier diode developed by Zhejiang University; (b) a commercial lateral GaN-on-silicon device A; and (c) a commercial lateral GaN-on-silicon device B with off-state bias (V_{OFF}) varying from 50 to 500 V.

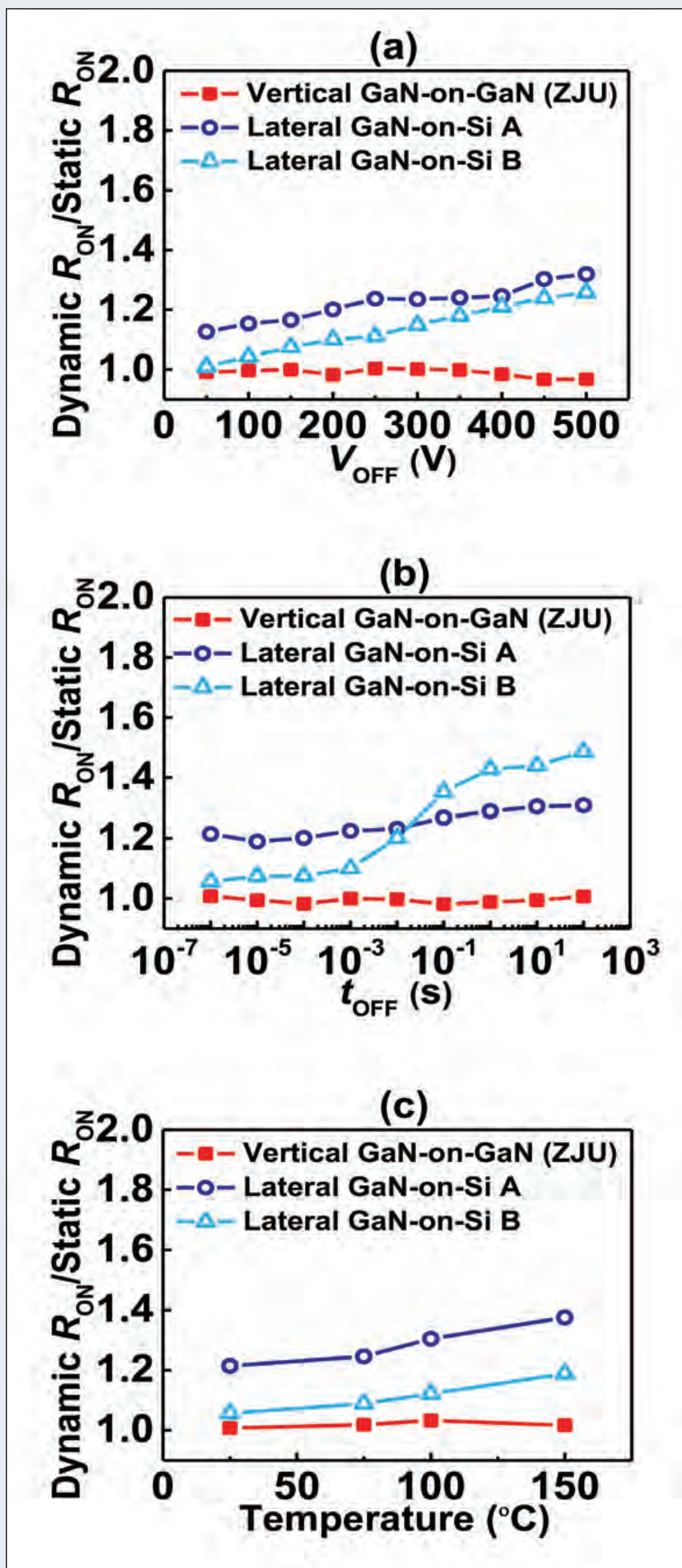


Figure 6. Dynamic R_{ON} of the three types of GaN devices extracted at only 200 ns after switching from: (a) varying off-state bias (V_{OFF}) up to 500 V, (b) t_{OFF} of 10^{-6}~10^{2} s and (c) high temperature up to 150 °C.

any surface- or buffer-trapping that will impair on the conductivity of the two-dimensional electron gas leads to a change in dynamic on-resistance.

Current-collapse-free performance

We have systematically and quantitatively evaluated the dynamic on-resistance under different switching conditions. Tests include: an off-state stress bias evaluation up to 500 V; an off-state stress time, over the range 10^{-6} s to 10^{2} s; and elevated temperatures of up to 150 °C. The higher off-voltages and longer off-state times in the tests could impose more severe stress on devices by inducing field-enhanced electron injection and accumulated charge trapping.

All of these tests demonstrate that our vertical GaN-on-GaN power rectifier is free from dynamic on-resistance degradation just 200 ns after switching from a high-voltage off-state, outperforming the state-of-the-art lateral GaN-on-silicon devices (see Figure 5 and 6).

This result is significant – it is the first time that there has been quantitative experimental verification that vertical GaN-on-GaN devices are capable of delivering a current-collapse-free performance and overcoming the grand challenge of dynamic on-resistance.

We attribute this superior dynamic performance to several strengths of the device. Firstly, as current flow is along the vertical direction, the diodes are inherently less susceptible to surface-trapping than cousins with a lateral architecture. In addition, there is minimal bulk trapping, thanks to the high crystalline quality in the homoepitaxial epilayers and the well-controlled background/compensation doping in the drift layer; and our nitridation-based termination technique can suppress edge leakage and enhance breakdown voltage through a favourable surface modification, rather than creating deep-level traps which could adversely influence the dynamic performance.

All these merits have helped our GaN-on-GaN devices to obliterate dynamic on-resistance degradation, a breakthrough that equips them with the potential to deliver high-efficiency and high-frequency energy conversion.

Further reading

S. Han *et al*. “Current-collapse-free and fast reverse recovery performance in vertical GaN-on-GaN Schottky barrier diode,” IEEE Transactions on Power Electronics, early access, DOI: 10.1109/TPEL.2018.2876444.

S. Han *et al*. IEEE Electron Device Letters **39** 572 (2018)

S. Yang *et al*. IEEE Transactions on Electron Devices **64** 5048 (2017)

The rise of GaN-based power systems – **Part II**

Part 1 of this series exploring gallium nitride (GaN) power devices provided a brief overview of GaN technology fundamentals, describing the growth of GaN power and its main application areas. This second part explores the technical details of applying GaN devices to implement innovative and highly efficient power conversion topologies.

By Paul Wiener, VP Strategic Marketing, GaN Systems

OBTAINING the optimum performance advantages of a GaN E-mode (enhancement-mode) high electron mobility transistor (E-HEMT) requires special design considerations, especially under dynamic conditions.

GaN has both lower switching and conduction losses, and its thermal performance provides many high-density power conversion possibilities. Unlike silicon (Si) MOSFETs, a GaN E-HEMT with no body diode has zero reverse recovery losses and exhibits high dv/dt ruggedness. This makes the technology an ideal fit for half-bridge hard switching designs. Meanwhile, both lower gate charge (Q_g) and output capacitance (C_{oss}) of GaN HEMTs make the performance of GaN-based soft-switching converters even better.

However, because of fast switching, circuit and layout techniques to minimize noise coupling and the Miller effect are more important than ever. With dv/dt> 100V/ns, GaN E-HEMTS switch faster than Si and silicon carbide (SiC) MOSFETs. GaN has four times faster turn-on and approximately two times faster turn-off time than a state-of-the-art SiC MOSFET with similar $R_{DS(on)}$. As a result, controlling noise coupling from the power to gate drive loop should be the first priority in circuit design. Also, high dv/dt and di/dt combined with low C_{ISS} and $V_{G(th)}$ require limiting gate spikes from going above the threshold or maximum rating under the Miller effect for safe operation since any added impedance that modifies the amplifier input impedance can cause problems.

Without proper design considerations, gate ringing or sustained oscillation may occur that can lead to device failure. This is more critical for 650 V hard switching half bridge applications since very high dv/dt spikes could occur at a hard turn-on. A single-ended topology is of less concern for the Miller effect. In addition, the design requirements on dv/dt and di/dt are relaxed for resonant zero voltage switching (ZVS) topology.

To minimize the Miller effect lowering the gate drive impedance (R_g and L_g) is critical, especially at turn-off. The basic rule is the gate needs to be held down as strong as possible with minimum impedance. The Miller effect is more prominent for 650 V-based than 100 V-based designs since the dv/dt is higher for the higher voltage design than in a lower voltage design. In addition, different design techniques are recommended for positive vs. negative dv/dt.

Positive dv/dt

- Prevent false turn-on
- Strong pull-down (low R_G/R_{OL})
- Low L_G to avoid ringing

Image 1. The 100 V GaN E-HEMT FB EVB (GS61004B-EVBCD) optimized for Class D amplifiers.

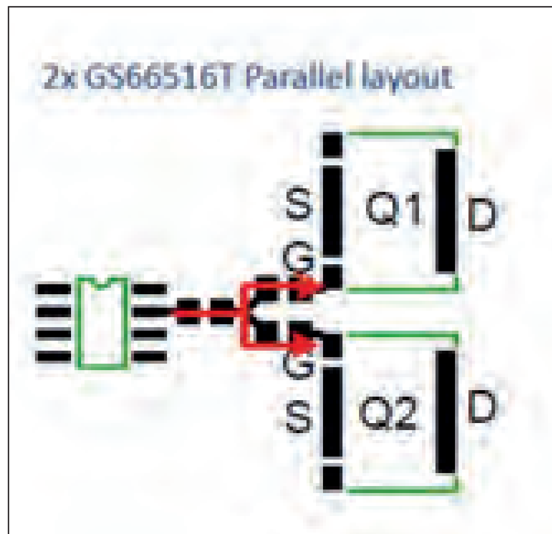


Image 2. Symmetry of dual gate drive in parallel design reduces PCB space.

- Use of negative gate bias at turn-off, -2 to -3V, helps

Negative dv/dt
- Occurs at turn-on of the complementary switch in half bridge
- Keep V_{GS-_pk} within -10 V
- Strong pull-down (low R_G/R_{OL}) and low LG for lower ringing
- V_{GS} may bounce back >0V (LC ringing), so ensure $V_{GS+_p}k< V_{G(TH)}$ to avoid false turn-on or gate oscillation

GaN E-HEMT speed can be easily controlled by gate resistors. A separate RG for turn-on and turn-off is recommended. For controlling the Miller effect, an $R_{G(ON)/RG(OFF})$ ratio ≥ 5 to 10 is recommended. For more details, please refer to the application guide "Design with GaN Enhancement mode HEMT" [1].

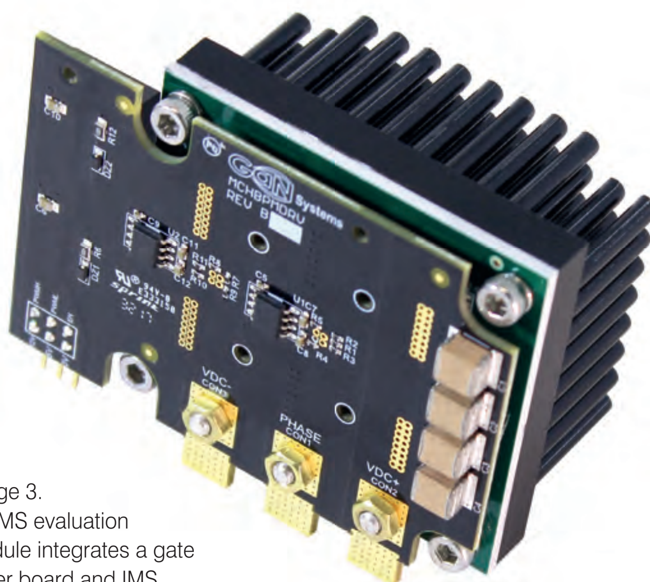


Image 3. An IMS evaluation module integrates a gate driver board and IMS PCB with a heatsink.

PCB layout

With their fast switching time, GaN E-HEMTs require the usual layout considerations to avoid gate ringing and oscillation. Suggested best layout practices for gate drives include:
- Physically separating the power loop and the drive loop areas to minimize noise coupling
- Minimizing the pull-down loop by locating the gate driver close to the ground capacitor
- Minimizing the turn-on (pull-up) loop by locating the VDD capacitor close to the driver
- Isolating and avoiding overlap between gate drive and drain copper pad
- Isolating and avoiding overlap from Drain/Source to control grounds

Several low (80-100 V) and high (650 V) voltage half/full bridges and gate driver/controller ICs from different suppliers have been verified to work with GaN E-HEMTs and simplify the implementation of best practices. Image 1 shows the GS61004B-EVBCD with a 60 V half-bridge GaN driver optimized for high frequency applications that include DC/DC conversion and wireless power charging.

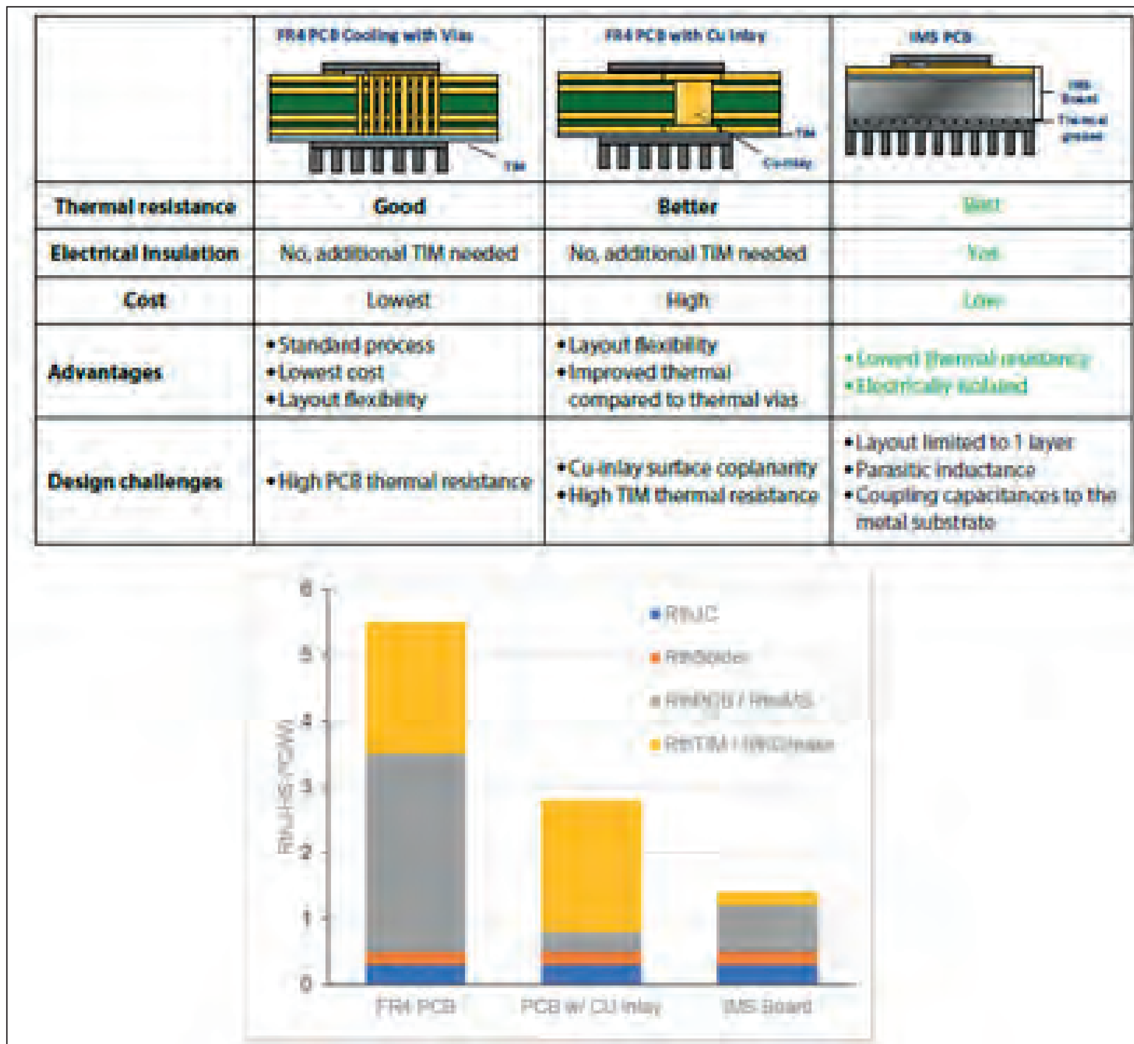
Paralleling techniques for GaN

GaN technology's $R_{DS(on)}$ and transfer characteristics, including transconductance that decreases with temperature, provide negative feedback to self-balance and compensate devices and overcome circuit mismatches. In addition to reducing the total gate drive loop in paralleling designs, a dual-gate drive makes it easier to have a symmetric gate drive layout and reduce the total layout footprint area. Image 2 shows the parallel layout for two GS66516T GaNPX packaged devices. The gate drive requirements for GaN are five to 10 times less than an equivalent Si MOSFET and have 50 times or greater lower gate drive losses at MHz-level switching.

Critical parasitic parameters can have a high impact on GaN paralleling. For that reason a star connection is recommended to equalize the gate/source inductances. Also, common source inductances should be minimized as much as possible. For high current parallel designs, a small negative gate drive turn-off bias (from -3V to -5V, synchronized) is recommended for lower turn-off losses and a more robust gate drive. The layout should have high frequency current flows occurring in opposite directions on two PCB layers for magnetic flux cancellation to lower parasitic inductances.

A high-power, GaN-based IMS platform

An insulated metal substrate (IMS) evaluation platform, the GSP65RxxHB-EVB, demonstrates the implementation of the design considerations discussed so far as well as others to achieve increased power density and reduce system cost with GaN power devices. The metal core/aluminum printed circuit board (PCB) with heatsink is shown in Image 3. Configured in half bridges, the IMS evaluation



	FR4 PCB Cooling with Vias	FR4 PCB with Cu Inlay	IMS PCB
Thermal resistance	Good	Better	Best
Electrical Insulation	No, additional TIM needed	No, additional TIM needed	Yes
Cost	Lowest	High	Low
Advantages	• Standard process • Lowest cost • Layout flexibility	• Layout flexibility • Improved thermal compared to thermal vias	• Lowest thermal resistance • Electrically isolated
Design challenges	• High PCB thermal resistance	• Cu-inlay surface coplanarity • High TIM thermal resistance	• Layout limited to 1 layer • Parasitic inductance • Coupling capacitances to the metal substrate

Image 4. Comparison of several design parameters including junction to heatsink thermal resistance (R_{thJ-HS}) for FR4 PCB with cooling vias and FR4 PCB with Cu inlay to an insulated metal substrate (IMS) board. Thermal results are estimated based on the GS66516B GaN E-HEMT.

modules are available in 2-4 kW and 4-7 kW power levels. The IMS module design approach has been used in automotive, industrial, server/datacenter, and consumer applications. Automotive applications include on-board chargers, DC/DC converters, three-phase inverters and high power wireless chargers. For industrial applications, the modules have been used in 3-7 kW photovoltaic inverters as well as energy storage systems (ESS) and motor drives, including variable frequency drives. Servers/datacenters have employed a 3 kW AC/DC power supply. Finally, IMS modules have been used in consumer/residential energy storage systems.
In contrast to thermal cooling for surface mount technology (SMT) packages that often use cooling vias or a copper (Cu) inlay, the IMS board provides several advantages as summarized in

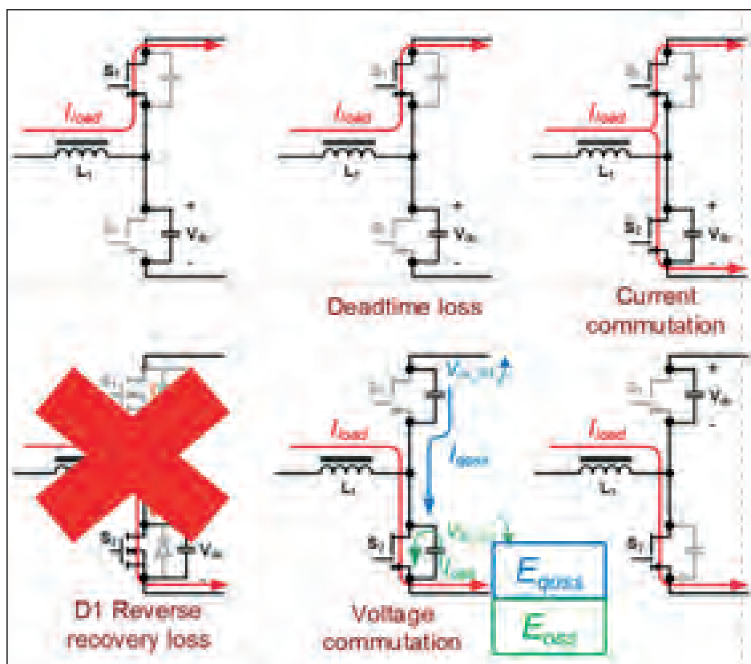
Switching transient and loss analysis of GaN

The hard-switching turn-on transition for GaN HEMTs is shown in Image 5. Compared to Si MOSFETs, the absence of reverse recovery loss means a relatively clean channel current Id waveform. A capacitive E_{qoss} loss is part of the hard-switching losses. For GaN HEMTs, the absence of the Q_{RR} makes the Q_{oss} noticeable although the value of the Q_{oss} for GaN HEMTs is still the smallest among both Si and SiC MOSFETs. The E_{oss} loss is introduced by the capacitance self-discharging current of the switch device itself and Eqoss loss is introduced by the capacitance charging current from the opposite switch device. Image 6 shows the difference between hard switching-on loss distribution in Si MOSFETs vs. GaN E-HEMTs.

Eon/Eoff scaling method for GaN

The E_{on} of GaN E-HEMTs depends on the junction temperature (T_j). Also, the devices from GaN Systems are highly scalable. As a result, an Eon/Eoff scaling method for GaN can be used to obtain the E_{on}/E_{off} at other operating conditions (different Vds, T_j, and R_g), by scaling the data from the initial operating conditions. Image 7 shows the step-by-step E_{on}/E_{off} scaling procedure.

This approach mainly requires three steps for both E_{on} and E_{off} scaling. For E_{on}, the first step is R_g scaling. Next is the E_{qoss} calculation and V_{ds} scaling. The third step is T_j scaling.



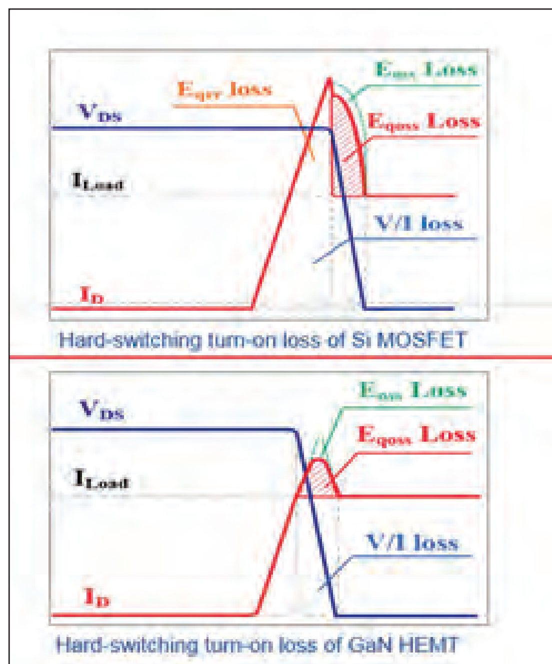


Image 6. No reverse recovery loss and lower capacitive loss mean lower E_{on} loss for GaN E-HEMTs.

Image 5. Hard switch-on transition and switch commutation principle of a GaN HEMT.

For E_{OFF}, the first step is R_g and T_j scaling, next is the E_{oss} calculation, and third is V_{ds} scaling. In this analysis, the initial condition is defined as V_{ds}=400V, $R_{g_}$on=10Ω, $R_{g_}$off=2Ω, and T_j=25°C. Note that the initial condition can be revised with an accurately measured E_{on}/E_{off} curve.

Dynamic R_{dson}

Trapping is a common problem in wide bandgap (WBG) semiconductors like GaN. It impacts the dynamic R_{DSon} (R_{dyn}) of GaN devices. While R_{dyn} reduces with higher junction temperatures due to the GaN E-HEMT's positive temperature coefficient, other factors that affect R_{dyn} include:

- Bias voltage
- Bias time
- Switching frequency
- Duty cycle

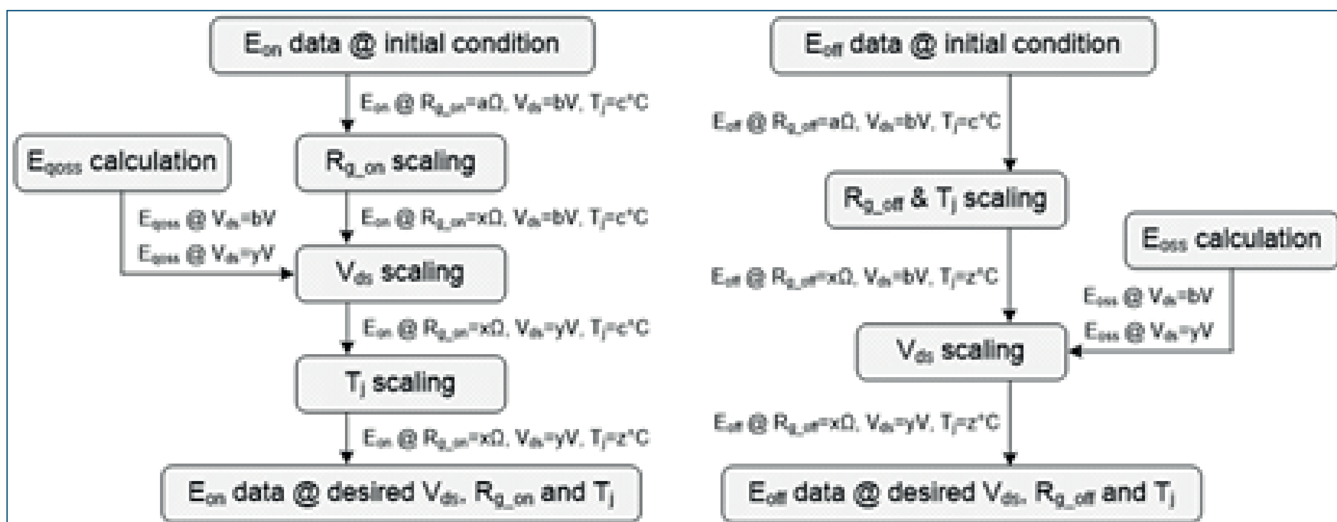
Image 7. E_{on}/E_{off} scaling procedure/ algorithm for GaN HEMTs.

It should be noted that dynamic $R_{DS(on)}$ effects are negligible in steady state operation.

Moving to GaN

With proper design considerations, designing engineers can build power systems that have one-quarter of the power loss, size, and weight of Si-based solutions at a fraction of the cost. This second in a series GaN article, identified and discussed several key product characteristics and circuit aspects toward achieving those results.

Editor's Note: Part III of this series by GaN Systems will discuss topologies based on gallium nitride technology as well as specific applications including wireless power.



Packaging solution for GaN on silicon power devices

Imec and UTAC co-developed a unique process for wafer thinning and backside metallization of highly stressed GaN-on-200 mm silicon wafers that enables a packaged 650V GaN device smaller than other 'state-of-the-art' approaches.

By Stefaan Decoutere and Nicolo Ronchi, imec

THE WIDE-BANDGAP material gallium-nitride (GaN) has many advantages over silicon (Si) when it comes to applications in the area of power electronics. With a higher breakdown strength and lower on-resistance, GaN-based power devices can convert power more efficiently than today's most advanced Si-based devices. Apart from these assets, GaN-based power devices have a 10 – 100 times faster switching speed than Si-based devices, which makes them perform significantly better at the system level. The first generation of GaN-based power devices have found applications thanks to these properties, such as battery chargers for mobile phones and electric cars, point-of-load power systems, industrial power supplies, DC/DC convertors for servers, and invertors for solar panel connections to the grid, to name a few.

Today, GaN is grown on a variety of substrates, including sapphire, silicon carbide (SiC) and silicon (Si). Silicon substrates are attractive because of the significantly lower cost perspective and the ability to use standard semiconductor processing lines. While industry is mainly working on wafers with diameters of 150mm for GaN devices, imec has pioneered the development of the technology on 200mm silicon wafers.

Fabricating GaN-on-Si power devices on 200mm wafers is however challenging: because of the larger diameter and targeted higher voltage range, wafer bowing can be a severe problem. The fundamental difficulty is caused by the mismatch in lattice and especially in the thermal expansion coefficient between the GaN/AlGaN layers and the silicon substrates. The AlGaN buffer, which is required to 'bridge' the silicon and GaN lattices, is grown at high temperatures. During cool down, the wafer gets warped, and the highly stressed wafers can easily break or exhibit micro-fractures. By careful stress engineering, imec has enabled a 200mm CMOS-compatible GaN power device platform. With this platform, enhancement-mode power switches and Schottky diodes can be developed for 100, 200 and 650 volt applications.

In addition to wafer fabrication, the presence of stress in the wafers also poses challenges during the packaging of these power devices. Although solutions exist for smaller-sized GaN-on-Si wafers, there is no reliable process for packaging brittle GaN-on-200mm devices. Without a packaging solution the development and migration of a GaN-on-200mm silicon technology is impossible. To tackle this challenge, imec collaborated with OSAT partner UTAC for the assembly of GaN on 200mm Si technology. Below, Stefaan Decoutere, Program Director GaN Power Electronics at imec, and Nicolo Ronchi, a researcher at imec, have teamed up with UTAC's R&D team to identify the challenges and to develop a process and bill of materials for the first, ultra-small, functional packaged GaN-on-200mm Si device.

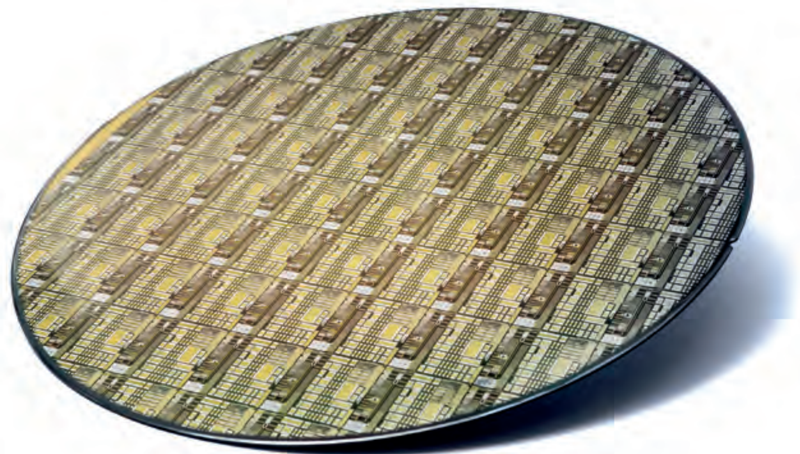


Figure 1. Typical 200mm Si wafer with processed GaN devices.

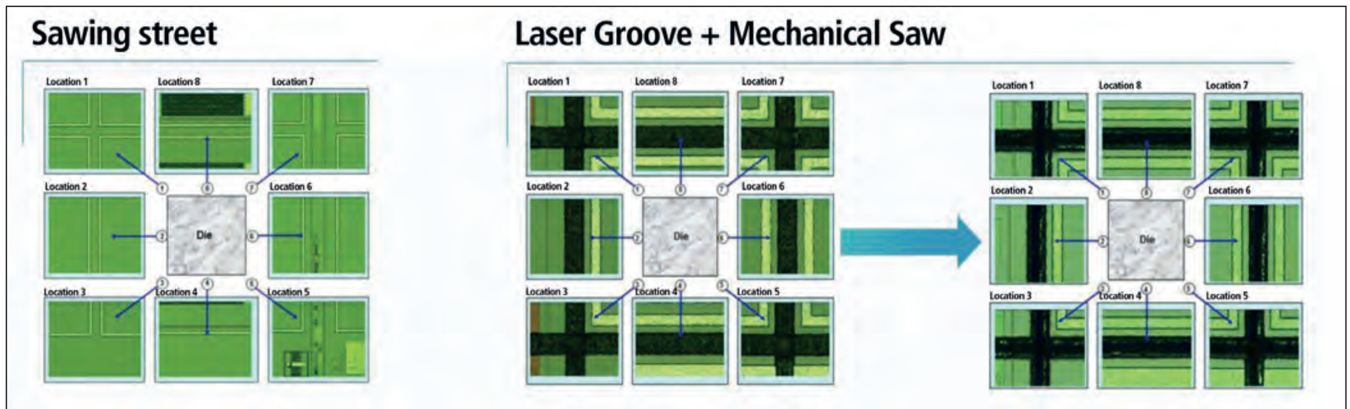


Figure 2. Illustration of the laser groove procedure and mechanical saw, resulting in limited chipping.

What are the challenges of packaging GaN-on-200mm silicon devices? Power devices typically operate at high voltages and high frequencies. In these devices, heat is being generated as a byproduct of operation. The package should therefore provide an efficient path for heat dissipation. For GaN-on-200mm silicon power devices, an attractive approach is to thin the silicon carrier wafer and subsequently apply back-side metallization. This way, a good thermal and electrical contact between the chip and the package can be established, and uniform heat dissipation can be guaranteed.

However, the tensile stress induced by the GaN layer on top of the 200mm silicon wafer is strong enough to bow the wafer. This can lead to breakage during wafer thinning and metallization. After successful backgrind and backside metallization of GaN-on 200mm wafers, dicing is required, and this process also presents its own set of challenges. Conventional sawing is not possible due to the brittle characteristics of the wafer; sawing can cause chipping and even micro-cracks. These issues can lead to premature device failure, pointing to the urgent need to define and optimize processing steps prior to packaging.

After dicing, the separated die need to be mounted into packages. These packages need to be as compact as possible, with an optimized short pin configuration. Compact packages and short pins will not only bring benefits for applications where size matters, they will also reduce the parasitic inductance that is typically caused by long bond wires and pins. This parasitic inductance is known to severely limit the final speed at which the packaged device can operate. A high thermal and electrical conductive material is also needed to ensure an efficient path between the die backside and the package which is essential for this type of package. Finally, the individual packaged devices will need to be soldered onto a PCB with good thermal conduction.

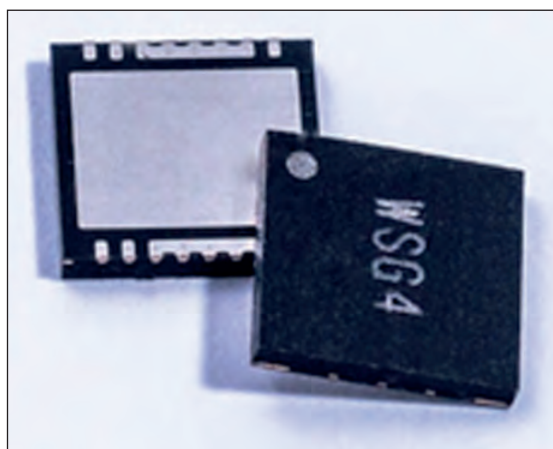


Figure 3. Picture of the 5x5mm^2 650V 16A packaged GaN device

A dedicated process flow

With these challenges in mind, imec and UTAC have developed a unique solution for packaging GaN-on-200mm Si power devices. For these developments, p-GaN high-mobility-electron devices (HEMTs) were processed on a thick (1,150μm) 200mm Si carrier wafer. On these wafers, a wafer warpage as large as 700 - 900μm was measured after wafer thinning (the warpage being the distortion from the lowest point to the highest point of the wafer), illustrating the difficulty of developing a reliable process flow.

Although there were no issues during wafer thinning, a high warpage post-backgrind process was observed. This is a high concern during the backside metallization of thinned wafers. UTAC together with their supplier worked on a backside metallization process addressing the high warpage after thinning, and successfully coated a Ti-Ni-Ag layer with a mirror finish. To decrease the level of chipping during die separation, UTAC defined a dicing process that includes laser grooving in conjunction with mechanical sawing. This combined process enables grooved trenches along the sawing streets prior to mechanical sawing. This also removes the GaN buffer along the die edges and results in limited chipping and cracking of the GaN buffer at the surface as a result.

In a final step, each die is mounted in an industry-standard dual flat no-lead (DFN) package. To meet the requirements for power applications, a highly conductive material was used at die attach, and small pins were provided.

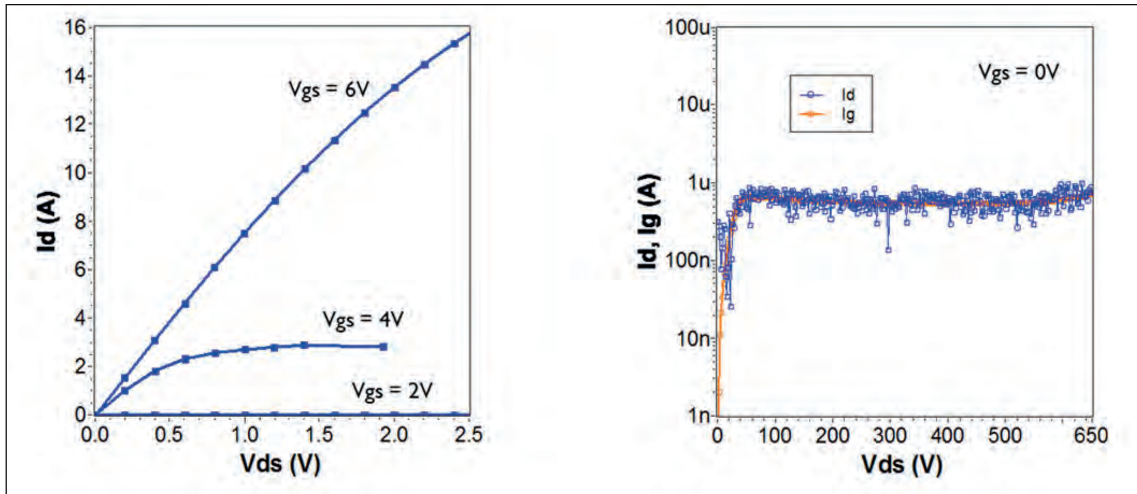


Figure 4. Electrical characterization of the packaged GaN-on-Si devices.

A fully functional, compact, 650V 16A GaN packaged device

With a total area of $5x5mm^2$ and a final thickness of 0.7mm, the resulting packaged devices are smaller than state-of-the-art (achieved using other techniques). To verify that they operate correctly, standard electrical characterizations were performed. It was found that the packaging process did not impact the operation or stability of the components. The DFN packaged devices can operate at voltages as high as 650V (drain-to-source breakdown voltage) and at 16A drain current, while exhibiting low inductance.

The GaN roadmap: new challenges for packaging

With this process flow, imec can now offer its GaN-on-200mm Si technology, all the way from GaN growth and processing to packaging. The packaged devices are available as standalone components and can be assembled as discrete components on a common PCB.

Further down the road, imec researchers are looking into other substrates besides silicon. They are exploring, for example, substrates that have a better matched coefficient of thermal expansion – such as the recently proposed QST® substrate from Qromis. This substrate promises to enable GaN power devices with operation beyond 650V. Alternatively, they are looking into SOI (silicon on insulator) as a substrate for GaN growth. This material, in combination with trench isolation, allows the monolithic integration of multiple GaN power devices onto a single chip, resulting in smaller and less complex overall systems. Using novel substrates will bring along additional challenges for packaging, which will be the subject of further research.

The research on GaN-on-SOI is part of imec's Industrial Affiliation Program for GaN power devices. Within this program, imec takes today's GaN-on-Si technology to a higher level of maturity and reliability, and explores new concepts for next-generation GaN technology.

The research is also carried out within the framework of the European ECSEL PowerBase project. The PowerBase project receives funding from the Electronic Component Systems for European Leadership Joint Undertaking under grant agreement No 662133.

Stefaan Decoutere

Stefaan Decoutere received his M.Sc. degree in Electronic Engineering and Ph.D. degree from the Katholieke Universiteit (KU) Leuven, Belgium, in 1986 and 1992 respectively. He has been with imec, Leuven, since 1987, where he started in high-voltage BCD technology development. From 1992 until 1997, he was in charge of the development of high-speed BiCMOS and SiGe HBT technologies. In 1998, he became the Head of imec's Mixed Signal/RF technology group. Since 2010 he has managed GaN power device technology development, and in 2015 he became director of the GaN technology program.

Nicolo Ronchi

Nicolò Ronchi was born in Thiene, Italy. He received the Laurea (masters) degree in Electronics Engineering and his PhD degree from the University of Padova, Italy, in 2008 and 2012, respectively. He started to work on GaN-based devices in 2007 during his master thesis work. His research activity on this technology continued during his PhD program and, since 2012, at imec in Belgium as a researcher in the Power and Mixed Signal Technologies group (PMST). His main interests include the characterization and reliability analysis of GaN-based semiconductor devices for high-frequency and power-switching applications.